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Adaptive Dual Fuzzy Sugeno-Driven Hybrid PWM for Robust Capacitor Voltage Balancing in T-Type NPC Inverters

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Abstract—This study presents an adaptive hybrid PWM control with dual fuzzy Sugeno control to improve a T-Type NPC inverter's capacitor voltage balancing. Using dual fuzzy Sugeno logic, the suggested approach optimizes both the modulating and carrier signals to maximize the inverter's performance under various operating conditions and modulation index fluctuations. Power quality is estimated by a grid-tied, three-level, three-phase T-type NPC inverter. In terms of the output line voltage THD and the fluctuation in the peak-to-peak dc-link capacitor voltage, test data reveal that the recommended hybrid PWM strategy outperforms standard PWM strategies Additionally, by lowering conduction and switching losses, the technique lessens the power switches' thermal stress, improving the inverter's dependability and efficiency. In MATLAB/Simulink 2024a, the suggested PWM approach is validated and analysed.

Index Terms—T-type neutral point clamped inverter, dual fuzzy sugeno, DC-link voltage imbalance, pulse width modulation, multilevel inverters, voltage source inverters, and total harmonic distortion.

I. INTRODUCTION

Several benefits over two level "voltage source inverters (VSIs)" have led to the widespread use of multilevel inverters (MLIs) in medium to high voltage applications and renewable solar photovoltaic (PV) systems. This includes reduced EMI, reduced filter size, reduced harmonic distortions, improved output waveform quality, etc. The three main topologies for MLIs are "neutral point clamped inverter (NPC)"[3], "fleeing capacitor inverter" (FC)[4], and "cascaded H-bridge inverter (CHB)"[5]. These characteristics include improved output voltage and current quality, flexibility, increased efficiency, and the capacity to handle voltage. However, in some situations, T-type NPC inverters—a partial variation of the NPC inverter topology—can outperform the NPC inverters in terms of efficiency [6]. Even though NPC inverters are well-known and offer appealing power quality, there are still certain difficult problems and opportunities for development. Total harmonic distortion, neutral point voltage imbalance, power loss, thermal stress, and other issues are the main obstacles.

These difficulties heavily depend on the PWM techniques used. The inverter's harmonic distortion, voltage balancing performance, power loss, and thermal stress may all be improved by using a suitable and carefully managed PWM approach. To address these issues, a number of enhanced PWM methods and control algorithms have been put forth in the literature.

II. LITERATURE SURVEY

[1] "F. Z. Peng, T. G. Habetler, and L. M. Tolbert", Transformer less multilayer power converters are discussed in this work as a potential use for electric motor drives with high voltage and/or power. With just fundamental frequency switching, multilevel converters may (1) produce near-sinusoidal voltages; (2) have virtually no common-mode voltage or electromagnetic interference; and (3) work well with high voltages and huge volt-ampere-rated motor drives. Since the cascade inverter uses multiple DC voltage sources, which can be derived from fuel cells or batteries, it is an ideal fit for large vehicle all-electric drives. The back-to-back diode-clamped converter works best in situations when there is an AC power source, like in a hybrid electric car. Simulation and experimental results show that these two converters are superior to two-level pulse width-modulation-based drivers.

[2]"S. P. Biswas, M. S. Anower, M. R. Islam, S. Mondal, S. M. Muyeen, and A. Ahmed", They suggested that this study provide a hybrid PWM approach. The proposed hybrid PWM technique introduces a modified modulating signal and a newly created carrier signal. The performance of the suggested hybrid PWM approach is assessed against RL load using a two-level VSI, both with and without filter conditions. Compared to current PWM techniques, Lower filtered voltage THD (0.89%) and filtered current THD (0.69%) are achieved by the proposed hybrid PWM technology. On the other hand, the proposed hybrid PWM approach shows "THDs of 12.50% for the inverter output current and 45.77% for the inverter output voltage", in filter-free conditions, which are likewise lower than those of current PWM systems. The proposed hybrid PWM technique further reduces the switching and conduction power losses of the VSI compared to existing PWM techniques. The MATLAB/Simulink environment is used to conduct the simulation work.

[3] "I. E. Lizama, P. K. Steimer, S. Bernet, and J. Rodriguez", The most popular modulation and control methods created to date are presented in this work in a fairly straightforward manner. The loss distribution in semiconductors is given particular consideration, and an active NPC inverter is proposed as a solution. The primary

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areas of application are covered in this paper along with a few technical issues including losses and capacitor balance.

[4]"S. Mondal, S. P. Biswas, M. R. Islam, and S. M. Muyeen"offer a solitary SC-based five-level transformer-less inverter. Only seven switches, a single capacitor, a single dc voltage source, and no diode are needed. The transformer-less MLI that is being suggested is also capable of auto-boosting. The inverter's switching losses are notably decreased because only three power switches are permitted to run at high frequency. Instead of employing a novel single SC based five-level transformer-less inverter topology, a control method is also proposed to inject a precisely controlled current into the grid that can govern both the active and reactive power support modes. There are also detailed comparisons between the suggested and state-of-the-art MLIs.

[5] "Babaei, E. A novel" multilevel converter topology with numerous stages and fewer power electronic switches is presented in this research. The sub multilevel converter blocks in the suggested circuit are connected in series. The best configurations of this topology are examined for a number of goals, including the smallest number of switches and capacitors as well as the lowest standing voltage on switches to generate the largest output voltage steps. Additionally, a new algorithm has been developed for determining the dc voltage sources psila magnitudes. According to simulation and practical results, the proposed topology reduces the number of switches, losses, installation space, and converter cost. Level multilevel converter have confirmed the functionality and performance of the suggested multilevel converter.

[6] "*M. A. Chaudhari and S. Srivastava"*, The purpose of this study is to compare and theoretically show the DC bus usage for a "Neutral Point Clamped (NPC)" three level inverter using the "Space Vector Pulse Width Modulation (SVPWM)" and "Sinusoidal Pulse Width Modulation (SPWM) techniques". When comparing SVPWM to SPWM, the linear region of the Modulation Index is used. Here, compared to the SPWM approach, the SVPWM technique exhibits lower Total Harmonic Distortion (THD). The results for an NPC three level inverter supplying RL load are modelled using MATLAB/SIMULINK.

III. PROPOSED METHOD

This paper suggests a well-balanced Hybrid PWM methodology that consists of a carrier signal and a modified modulating signal.

I. ADOPTED INVERTER TOPOLOGY

A three phase 3-L grid connected T-type neutral point clamped Inverter is depicted in Fig. 1.

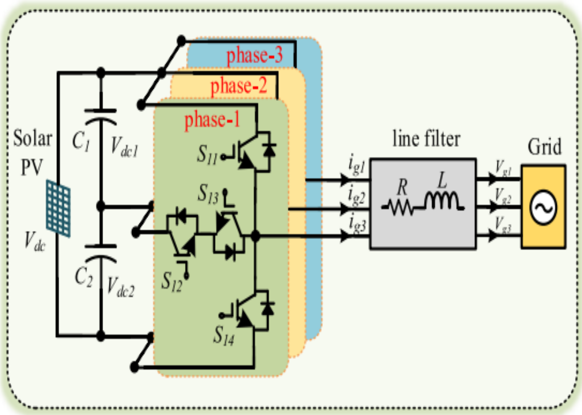

Fig 1. 3-phase, 3-level, grid-connected T-type NPCI inverter topology powered by solar PV.

The input side of the inverter, which is powered by a solar PV, uses two dc-link capacitors (C1, C2). The twelve power switches that make up the inverter are "S11, S12, S13, S14, S21, S22, S23, S24, S31, S32, S33, and S34". Four power switches are required for each phase. It is definitely forbidden to turn on switch pairs "S11, S13, and S12, S14" simultaneously in order to prevent inverter failure because they are known to be each other's opposites. The output side of the inverter is connected to the grid via an RL line filter to lower the harmonics of the current and line voltage.

II. CLOSED-LOOP CONTROL STRATEGY

For the chosen inverter topology, which can provide the grid with both active and reactive power, Fig. 2 shows a typical grid linked do reference frame based closed-loop control method. To match with the grid voltage reference frame, the three-phase AC current and voltage signals are transformed into D (direct) and Q (quadrature) components, which stand for active and reactive power, respectively. The phase locked loop (PLL)determines the α and β values with the phase angle of the voltage and current, respectively, by sensing the grid voltage (Vg) and grid current (ig). Id and iq, the measured direct and quadrature axis components of the grid current, respectively, can be used to individually manage active and reactive power. The measured errors are then supplied to the PI controller after id &iq are compared with the reference quantities i∗ d &i∗ q, respectively. Two at the output The three phase reference signals are created by converting the reference signals (Md and Mq) from the dq frame to the abc frame. The suggested modulating signal of the hybrid PWM approach is then created by further altering these reference signals.

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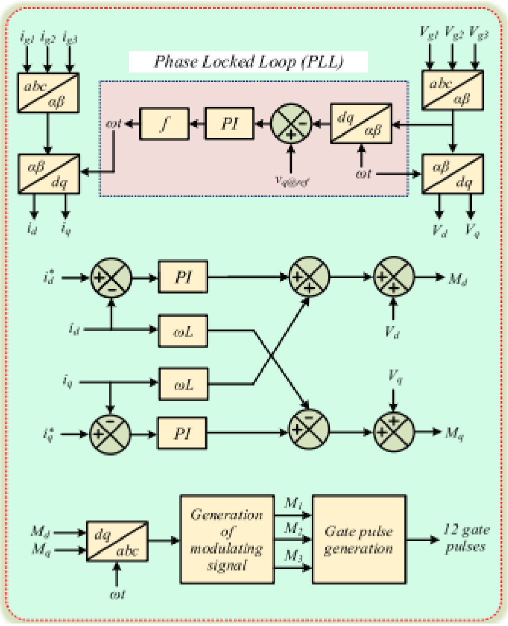

Fig 2. Closed-loop control strategy for the adopted inverter topology.

III. DUAL FUZZY-SUGENO METHOD

The Dual Fuzzy-Sugeno Method provides enhanced decision-making and control by integrating two Sugeno-type fuzzy inference systems (FIS). The approach is especially convenient when dealing with complex systems that have nonlinear dynamics and uncertain parameters.

Working Mechanism:
Input Receipt – The system receives numerical or linguistic inputs like sensor measurements.
Parallel Fuzzification – Both Sugeno models transform crisp inputs into fuzzy sets using different membership functions.
Rule Application – Every Sugeno system possesses independent if-then rules.
Output Calculation – Outputs are computed by weighted averages or linear functions.
Aggregation & Final Output – The two outputs are weighted and combined to create resulting exact final decision or control signal.
Major benefits:
Increased Robustness – Best able to handle uncertain and nonlinear behaviour compared to other control methods.
Flexibility – Reacts in an adaptive manner under changing input conditions.
Improved Decision-Making – Takes into account a number of different views, giving better and informed outcomes.
Flexibility – Combines qualitative and quantitative data to facilitate wider applications in robotics, automation, and process control.
Through the union of two different Sugeno models, the approach promises to offer a stronger, more flexible, and more effective solution to real-world decision-making problems.

IV. PROPOSED HYBRID PWM TECHNIQUE DEVELOPMENT

The core components of the suggested hybrid PWM approach are the carrier signal and the modified modulating signal. The procedures for creating the suggested modified carrier signal, modulating signal, and gate pulses needed for the power switches are briefly explained in this section.

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A. GENERATING THE MODULATING SIGNAL

A triangle signal and three sinusoidal signals with varying amplitudes are combined to create the suggested modified modulating signal. Fig.3shows the process of creating the suggested modified modulating signal, Mp. Initially, a sinusoidal signal (P) is obtained with a frequency three times greater than the fundamental, so that:

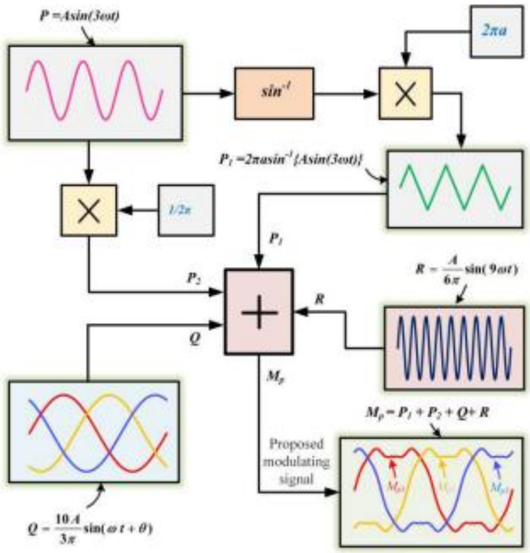

Fig 3. The process by which the modulating signal for the suggested hybrid PWM approach is generated.

$$P = A\sin\ (3\,\omega\, t)$$

where A and ω stand for the signal's amplitude and angular frequency, respectively. With the help of the sinusoidal signal (P),

PWM Technique	Mathematical Representation
SPWM [7]	$Y_1 = A\sin(\omega t + \theta)$ $[Y_{11}\quad Y_{12}\quad Y_{13}] = [Y_{1_{\theta=0^\circ}}\quad Y_{1_{\theta=-120^\circ}}\quad Y_{1_{\theta=120^\circ}}]$
CSVPWM [8]	$Y_2 = \frac{2}{\sqrt{3}}\{A\sin(\omega t + \theta)\} - \frac{1}{2}\{\max(Y_{11}, Y_{12}, Y_{13})\}$ $+\frac{1}{2}\{\min(Y_{11}, Y_{12}, Y_{13})\}$ $[Y_{21}\quad Y_{22}\quad Y_{23}] = [Y_{2_{\theta=0^\circ}}\quad Y_{2_{\theta=-120^\circ}}\quad Y_{2_{\theta=120^\circ}}]$
THPWM [9]	$Z = cA\sin(\omega t + \theta)$ $Y_3 = A\sin(\omega t + \theta) + Z$ $[Y_{31}\quad Y_{32}\quad Y_{33}] = [Y_{3_{\theta=0^\circ}}\quad Y_{3_{\theta=-120^\circ}}\quad Y_{3_{\theta=120^\circ}}]$
SDPWM [10]	$Y_4 = \frac{2}{\sqrt{3}}[A\sin(\omega t + \theta)] + \frac{1}{2\pi}[A\sin(3\omega t + \theta)]$ $+\frac{1}{60\pi}[A\sin(9\omega t + \theta)] + \frac{1}{180\pi}[A\sin(15\omega t + \theta)]...$ $[Y_{41}\quad Y_{42}\quad Y_{43}] = [Y_{4_{\theta=0^\circ}}\quad Y_{4_{\theta=-120^\circ}}\quad Y_{4_{\theta=120^\circ}}]$

TABLE 1. Mathematical depiction of many PWM methods.

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B.Modulation of Space Vector Pulse Width (PWM)

We use various technologies to generate waveforms that work well for both input and output. Different switching techniques lead to unique outcomes that can be useful in the business world. There are numerous switching modulations for multi-level inverters. Analysing each of these characteristics is crucial to meeting industry demands. The pattern of SVM switching improves the inverter's dynamic performance.

"Space Vector Modulation (SVM)" is a vector method for three-phase inverters using "Pulse Width Modulation (PWM)" technology. An AC signal produced by the inverter gives the motor load a high voltage with less overall harmonic distortion. The basis of "space vector pulse width modulation" (SVPWM) is vector selection in the q-d stationary reference frame. It follows of equation defines the commanded voltage vector. Plotting of the commanded vector and the vectors that the inverter can obtain is done. At some point in time, the intended vector Vs*qds is displayed; however, if a three-phase set of voltages is needed on the load, it will take a circular route. Finding the three closest vectors is the first stage in the SVM scheme.

$$v_{qs}^{s*} = \frac{2}{3}v_{ag}^{*} - \frac{1}{3}v_{bg}^{*} - \frac{1}{3}v_{cg}^{*}$$

Space Vector Concept

The circuit model of a typical three-phase voltage source PWM inverter is shown in Fig. 4The six power switches that make up the output, S1 through S6, are controlled by the switching variables a, a′, b, b′, c, and c′When an upper switch is turned on, i.e., when a, b, or c is 1, the matching lower transistor is turned off, resulting in aC, b′, or c′ being 0. Therefore, by using the on and off states of higher switches S1, S3, and S5, the output voltage may be determined. SVPWM modulation differs from PWM modulation.

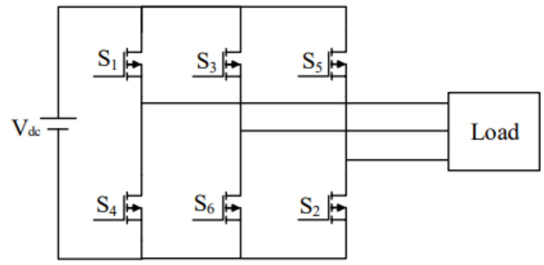

Fig 4.Inverterwith a source of three-phase voltage

In this modulation technique, the three phase quantities can be transformed into the matching two-phase quantities in a synchronously rotating frame or a stationary frame. These two-phase components can be utilized to calculate the reference vector magnitude, which is used to regulate the inverter output. The following section describes how to get the rotating space vector while accounting for the stationary reference frame.

There are six switching states for the 180° style of operation in addition to two additional states that turn on all three upper arm or lower arm switches. To encode these eight states in binary (one-zero encoding), three bits are required (23 = 8). You only need to indicate the status of either the upper or lower arm switches since they always work together in a complementary way. To turn on an upper switch (i.e., a, b, or c is set to "1"), the corresponding bottom switch is turned off. Eight distinct on/off pattern combinations exist for the three upper transistors (S1, S3, and S5).The vectorvoltages are [a, b, c], and also the line-to-line vectorvoltages is [Vab Vbc Vca].

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

Line to neutral (phase) voltage vector $[V_{an}\ V_{bn}\ V_{cn}]^t$

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 0 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

figure5. displays the eight indicator voltage vectors (V0 to V7).

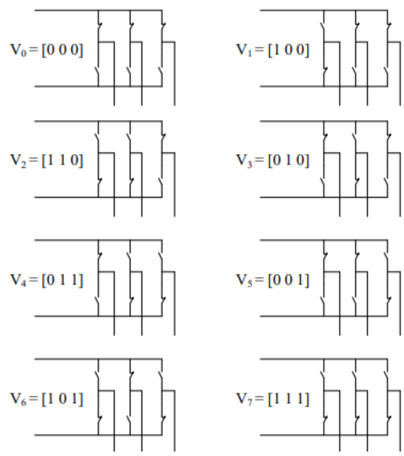

Fig 5. vector inverter voltage

Table 2 below displays the output line-to-line voltages, phase voltages, and eight combinations

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

Table 2The outputs of line-to-line voltage and phase voltages of SVPWM.

Principle of Space Vector PWM

In space vector PWM, we can think of the sinusoidal voltage as a steady amplitude vector that's spinning at a constant frequency. This PWM method uses a mix of

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eight different switching patterns (V0 to V7) to get as close as possible to the target reference voltage, Vref. Space vector PWM helps in transforming coordinates, switching from the abc reference frame to the stationary d-q frame. We translate a three-phase voltage vector into a vector in the stationary d-q coordinate frame to illustrate how we depict the total quantity of three-phase voltage. The plane is split into six sections, each covering 60 degrees, with the vectors V1 through V6 marking the boundaries.Two adjacent non-zero vectors and two zero vectors combine to form Vref.

Fundamental Sectors and Vectors for Switching

The six active vectors in Figure 3.10 are “V1, V2, V3, V4, V5, and V6”. The load receives a DC voltage. 60 degrees are covered by each sector (1–6). (V0, V7) are two vectors with zeros. They can be found in the place of origin. The load receives no voltage.

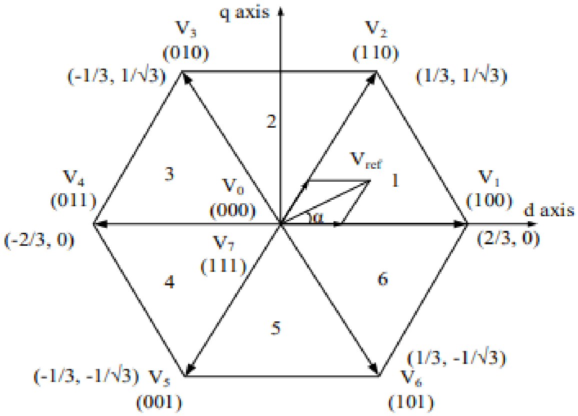

Fig 6. Simple sectors and vectors for switching

Understanding Space Vector PWM

Step 1: First, figure out the angle (α), alongside Vd, Vq, and Vref.

Step 2: Next, calculate the periods T1, T2, and T0.

Step 3: Finally, determine the switching times for each transistor (from S1 to S6).

1.

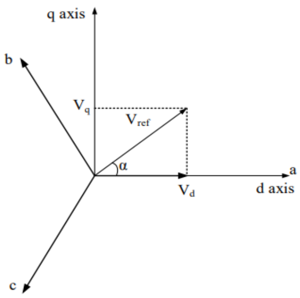

Fig 7.elements of the vector of voltage space in (dp).

Understanding angle (α), Vd, Vq, and Vref

In Fig. 7, you can see how the voltage space vector and its parts come together to calculate thevoltage of direct axis Vd, voltage of quadrature axis Vq, angle α, and reference voltage Vref.

$$V_d = V_{an} - V_{bn}\cos 60 - V_{cn}\cos 60$$

$$= V_{an} - \frac{1}{2}V_{bn} - \frac{1}{2}V_{cn}$$

$$V_q = 0 - V_{bn}\cos 30 - V_{cn}\cos 30$$

$$= 0 + \frac{\sqrt{3}}{2}V_{bn} - \frac{\sqrt{3}}{2}V_{cn}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}$$

$$|\overline{V}_{ref}| = \sqrt{V_d^2 + V_q^2}$$

$$\alpha = \tan^{-1}\left(\frac{V_q}{V_d}\right) = \omega_s t = 2\pi f_s t$$

The fundamental frequency (fs) is an important concept here. Let's break down the duration of the switching time at sector 1. We'll go over how to determine the time durations T1, T2, and T0.

$$\int_0^{T_s}\overline{V}_{ref} = \int_0^{T_1}\overline{V}_1 dt + \int_{0}^{T_1+T_2}\overline{V}_2 dt + \int_{T_1+T_2}^{T_s}\overline{V}_0$$

$$T_s \cdot \overline{V}_{ref} = (T_1 \cdot \overline{V}_1 + T_2 \cdot \overline{V}_2)$$

$$T_s \cdot |\overline{V}_{ref}| \cdot \begin{bmatrix} \cos\alpha \\ \sin\alpha \end{bmatrix} = T_1 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_1 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} \cos(\pi/3) \\ \sin(\pi/3) \end{bmatrix}$$

where $0 \le \alpha \le 60°$

$$T_1 = T_s \cdot \frac{|\overline{V}_{ref}|}{\frac{2}{3}V_{dc}} \cdot \frac{\sin\left(\frac{\pi}{3} - \alpha\right)}{\sin(\pi/3)}$$

$$T_1 = \sqrt{3}T_s \frac{|\overline{V}_{ref}|}{V_{dc}} \cdot \sin\left(\frac{\pi}{3} - \alpha\right)$$

$$T_2 = T_s \frac{|\overline{V}_{ref}|}{\frac{2}{3}V_{dc}} \cdot \frac{\sin(\alpha)}{\sin(\pi/3)}$$

$$T_2 = \sqrt{3}T_s \frac{|\overline{V}_{ref}|}{V_{dc}} \cdot \sin(\alpha)$$

$$T_0 = T_s - (T_1 + T_2)$$

Switching time duration at any sector is shown below

$$T_1 = \sqrt{3}T_s \frac{|\overline{V}_{ref}|}{V_{dc}} \cdot \left[\sin\left(\left(\frac{\pi}{3} - \alpha\right) + \left(\frac{n-1}{3}\pi\right)\right)\right]$$

$$T_1 = \sqrt{3}T_s \frac{|\overline{V}_{ref}|}{V_{dc}} \cdot \sin\left(\frac{n\pi}{3} - \alpha\right)$$

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$$T_1 = \sqrt{3}T_s \frac{|V_{ref}|}{V_{dc}} \cdot \left[\sin\frac{n\pi}{3}\cos\alpha - \cos\frac{n\pi}{3}\sin\alpha\right]$$

$$T_2 = \sqrt{3}T_s \frac{|V_{ref}|}{V_{dc}} \cdot \left[\mathrm{Sin}\left(\alpha - \frac{n-1}{3}\pi\right)\right]$$

$$T_2 = \sqrt{3}T_s \frac{|V_{ref}|}{V_{dc}} \cdot \left[\sin\alpha\cos\frac{n-1}{3}\pi - \cos\alpha\sin\frac{n-1}{3}\pi\right]$$

$$T_0 = T_s - T_1 - T_2$$

where, n=1 through 6 (that is sector 1 to 6), $0 \le \alpha \le 60°$ (note: Ts=Tz)

IV. GENERATING GATE PULSE

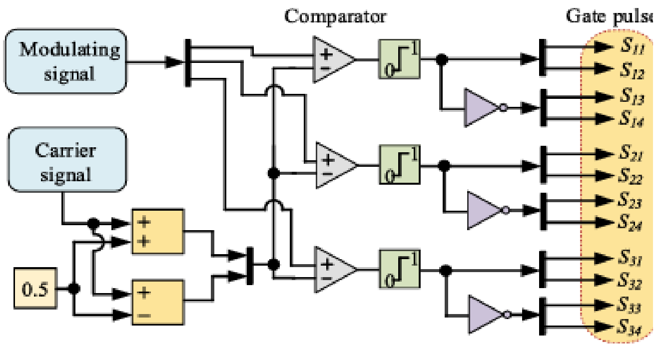

Fig 8. The gate generation process for adapted topology.

The gate pulse generating process of a certain inverter topology is depicted in fig.8 above, which is related to your research on T-Type NPC inverters. Here is a summary of its main elements.

1. Modulating Signal & Carrier Signal

They are the PWM inputs. Modulating signal is the AC output reference, whereas the carrier signal is a high-frequency wave for comparison.

2. Comparators

They contrast the modulation signal with the carrier signal. The output may be high or low, depending on how much stronger the modulating signal is than the carrier signal.

3. Blocks of Logic and Processing

Thresholding operations (and maybe fuzzy logic in your situation) and the logic gates.0.5 is a value being used as a reference, maybe for biasing or centring the signal.

4. Gate Pulse Output

Signal processing is utilized to send the signals to the inverters and logic gates in order to generate precise gate pulses ($S_{1\ 1}$ to $S_{3\ 4}$).The switching of transistors in the T-Type NPC inverter is controlled by the pulses for voltage balancing. Usage in Your Project Context. The configuration explained supplies balanced voltages to the capacitors via dynamic regulation of the PWM method.

Double fuzzy Sugeno-driven hybrid PWM most probably changes the modulation process for enhanced robustness in capacitor voltage balancing. Gate pulsing of output controls power semiconductor switches to ensure proper inverter operation.

IV. SIMULATION RESULTS

The proposed controller is simulated in different conditions i.e, three phase No- load and Step change in Load.

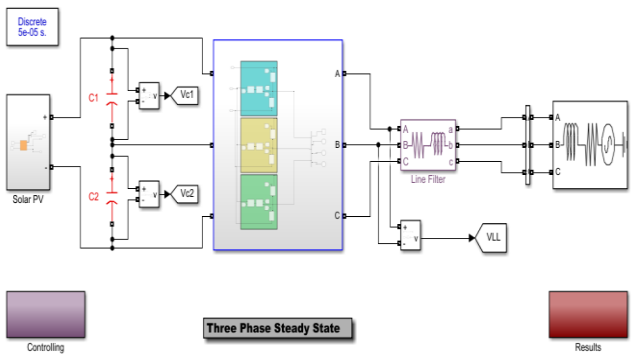

Fig 9.Solar PV fed grid-connected3-phase, 3-level T-type NPC Inverter topology.

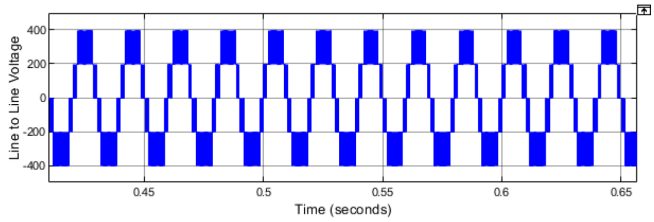

Fig 9(a).Line voltage of inverter output

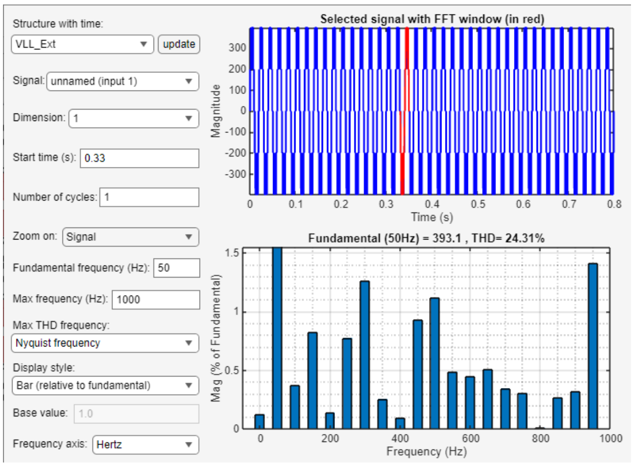

Fig 9(b).line voltage of Inverter output THD spectrum

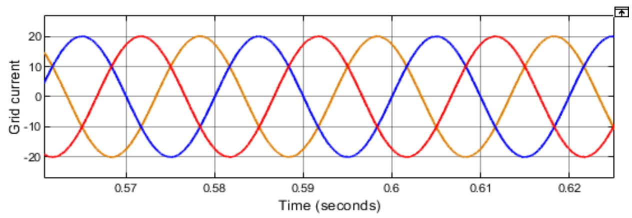

Fig 9(c). grid current

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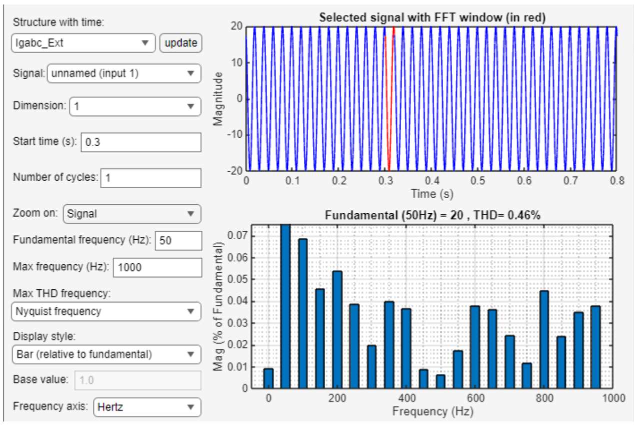


Fig 9(d).Grid current THD spectrum using the suggested hybrid PWM method

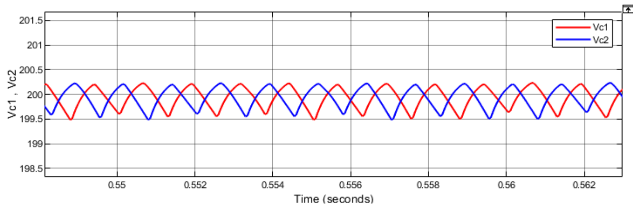
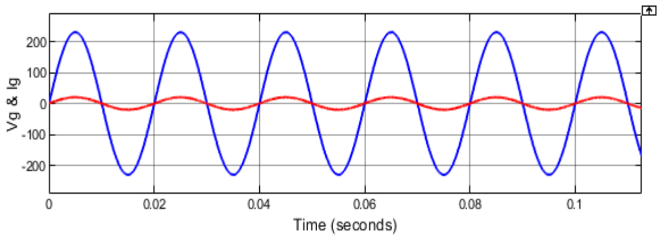
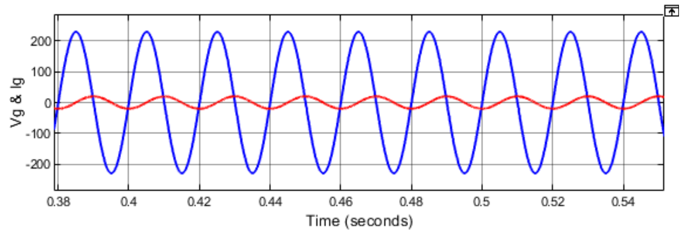


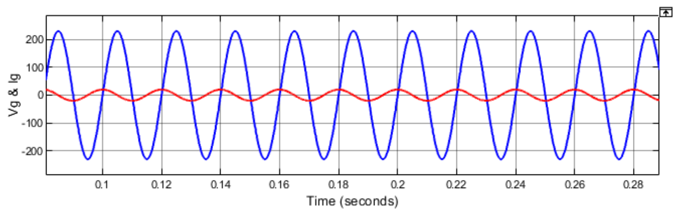
Fig 9(e).voltage differential in the dc-link capacitor under the suggested hybrid PWM approaches



(a)



(b)



(c)

Fig 10. Waveforms of grid current and voltage at (a) unity (b) lagging and (c) leading power factor.

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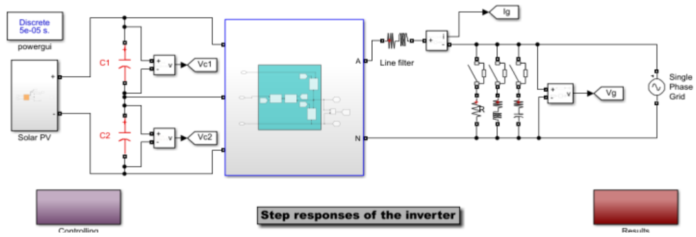

Fig 11.step response circuit

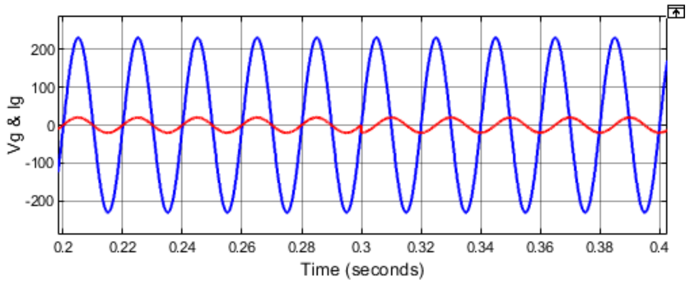

Fig 11(a). 1st Step change from resistive to Inductive

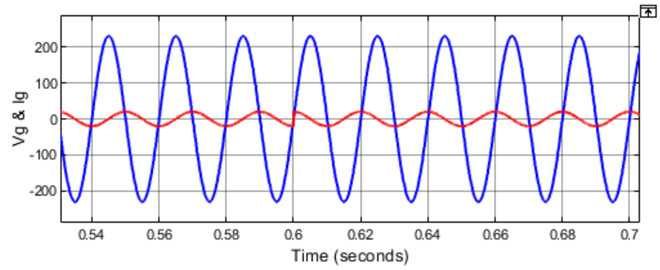

Fig 11(b). 1st Step change from Inductive to capacitive

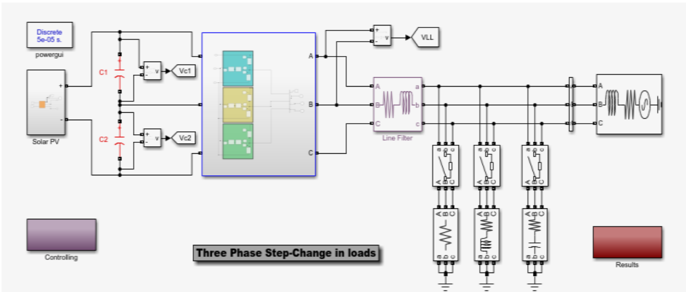

Fig 12. Step change in loads

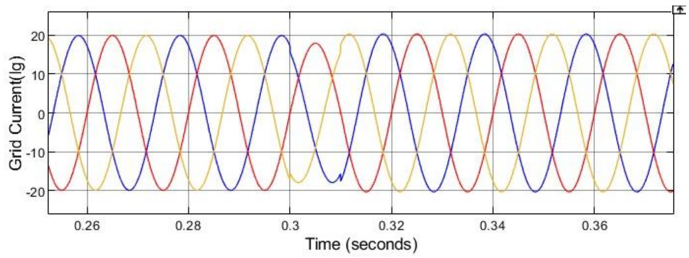

Fig 12(a). Grid voltage and grid current waveform at 3 phase

VI. CONCLUSION

The hybrid PWM approach reduces the junction temperature caused by power loss, hence effectively reducing the thermal stress on power switches. The

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simulation results show that the total harmonic distortion (THD) of both the line output voltage and the difference in the dc-link capacitor voltage has improved a lot with the new hybrid PWM approachThe recommended technique's durability and effectiveness are further guaranteed by the strong connection between the simulated and experimental outcomes. Ultimately, adopting double fuzzy Sugeno control in an adaptive hybrid PWM strategy is the best option for solar PV grid-tied systems when compared to other PWM techniques.

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