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HYBRID FULL SUBTRACTOR CIRCUIT USING FULL SWING XOR-XNOR CELL

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Abstract— The full subtractor circuit plays a vital role in the design of arithmetic circuits. In this article, a low power, high speed arithmetic circuits using full swing XOR-XNOR cell was proposed. The proposed circuit reduces the delay upto 41%. The performance of the proposed circuit can be measured by simulating it in tanner tool software.

Keywords —Full Subtractor,XOR,XNOR,Full Swing.

I.INTRODUCTION

The Full Adder is designed in a single module using MOS transistors. The complementary CMOS Full Adder is an example. The selected design uses 28 transistors to realize pull-up and pull-down networks of the FA. It provides full swing outputs and robustness against voltage scaling and transistor seizing. The main drawback of this circuit is high input capacitance as each of the inputs is connected to the gates having at least a PMOS and an NMOS transistor which degrades the speed of the adder. In the classical approach, FA can also be designed using pass transistors. However, the pass transistor have an inherent threshold voltage drop problem. When logic "1" and logic "0" is passed through NMOS and PMOS respectively, full swing logic "0" and logic "1" are not obtained at the output. To resolve the issue, a transmission gate (TG)-basic approach has been developed. In this style, an NMOS transistor and PMOS transistor are connected in parallel and controlled by complementary control signals. These PMOS and NMOS are turned on simultaneously and provide paths to both logic (logic "1" and logic "0") to provide full swing output. TG-based adder consumes low power however, it has weak driving capacity. Performance of this circuit can be enhanced by using the buffer at the output.

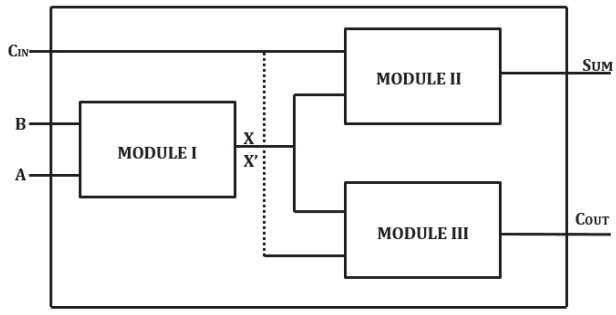

Fig.1. Full Adder Block Diagram

As shown in the Fig.1, Module I generates full swing XOR and XNOR outputs of two input signal (A and B) simultaneously. These XOR-XNOR signals must have good driving capabilities as these signals have to drive other two modules. Module II and the Module III is the sum and the carry circuit which provides the sum and carry outputs (COUT), respectively, using the output of Module I and third input signal (CIN). The main advantage of the hybrid style is that all the modules can be optimized at the individual level, and the number of transistors can be reduced, which reduces the internal power dissipation nodes. The performance of hybrid style FA is a good as a single unit or small chains, however, they lack driving capabilities in higher bit address implemented through cascading stages.

Performance of XOR-XNOR circuit plays a vital role in the performance of hybrid FA design. Various approaches to designing XOR-XNOR circuits can be presented in recent years. These approaches can be broadly classified into two categories. In the first approach, the XOR circuit is synthesized initially, and then XNOR output is generated using an inverter. This approach has a drawback that XOR and XNOR outputs are not generated simultaneously, which increase the chance of generating false switching and glitches in the output of the modules II and III. In another approach, the XOR-XNOR circuit is designed such that the XOR and XNOR outputs are generated simultaneously. In this approach, the delay difference between XOR and XNOR signals is tried to be minimized. An XOR-XNOR circuit using CPL gives the simultaneous generation of XOR-XNOR outputs. The output voltage level in the circuit is recovered using the feedback transistor. In digital circuits, circuits are the most critical components used in processor of portable devices, full subtractor is a combinational digital circuit that performs 1-bit subtraction with borrow-in. Subtractors are useful for Digital Signal Processing and networking based systems. The full subtractor generates two output bits: the difference and borrow out. There are two types of subtractors: half subtractor and full subtractor. In this paper we have used full subtractor. In the proposed circuit there are 22 transistors which reduce the delay. The complementary pass transistor logic (CPL) provides high speed, full swing output and good driving capabilities because of high speed differential stage. The Arithmetic circuits are extensively used in the data paths consuming almost one third of power in the high performance of microprocessors. Therefore it can enhancing the performance for improving the whole system significantly. To realize a full subtractor(FS) circuits, several static

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CMOS logic style have been presented. These logic style can be broadly classified into two categories: 1) Classical design 2) Hybrid design. The classical design is a single module MOS transistor, the hybrid design is divided into three modules. In the circuit there are three modules: they are Module 1 which generates full swing XNOR-XNOR output of two input signals. The Module 2 is the difference circuit and the Module 3 is the borrow circuit. In the block diagram of the full subtractor we have used these three modules, the input to the module 1 is A and B as it generates the XOR-XNOR outputs. The input to module 2 is the Bin and the

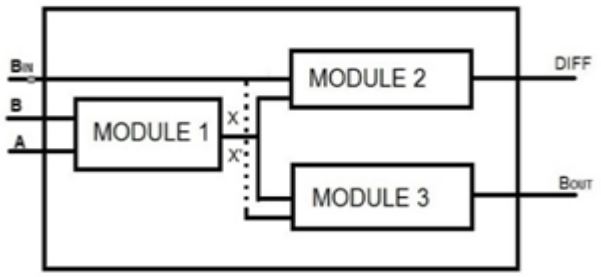

Fig.2. Block diagram of FS circuit

Module 2: Module 2 can be implemented by considering Bin and the outputs of the XOR-XNOR circuit as input signal. The most important prerequisite of this module is to provide enough driving power to the following gates:

DIFF=(A ⊕ B) ⊕ CIN+ (A ⊕ B)'⊕ CIN.

Module 3: The third module of the FS is the Borrow circuit(Bout). Output borrow of the full subtractor can be calculated using XOR-XNOR outputs of the module 1 and the previous carry DIFF. In cascading systems, delay of this module effects the overall delay most as the output of this module depends upon the output borrow of the previous FS.

Bout= (A⊕ B')DIFF+ (A⊕ B)A'

III.PROPOSED XOR-XNOR CIRCUIT

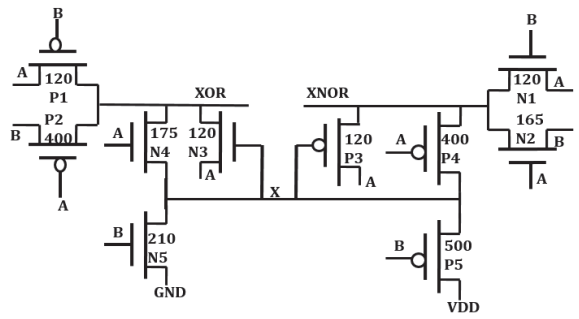

Fig.3. Propose XOR-XNOR circuit for Full Adder

The propose XOR-XNOR circuit using ten transistors (10-T) is shown in the figure. The proposed XOR-XNOR circuit is based on CPL and cross coupled structure. It uses two PMOS (P1 and P2) and three NMOS (N3, N4 and N5) transistor at the XOR output side and two NMOS (N1 and N2) and three PMOS (P3, P4 and P5) at the XNOR output side. At the XOR side, P1 and P2 are connected in parallel as PTL, N4, and N5 as a restorer to provide a full swing output and N3 as feedback transistor. Similarly, at the XNOR output side N1 and N2 transistors are connected in parallel PTL, P4, and P5 as the restorer to provide a full swing output and the P3 as a feedback transistor.

Table 1: Charging and discharging paths for the different input combinations in the proposed XOR-XNOR circuit.

Inputs AB	Path		Path	
	XOR (Full Swing)	XOR (Partial Swing)	XOR (Full Swing)	XNOR (Partial Swing)
00	N3	P1, P2	P4, P5	-
01	P2	-	N1	P4, P3
10	P1	N4, N3	N2	-
11	N4, N5	-	P3	N1,N2

For understanding the operation of the proposed design, charging and discharging paths for XOR and XNOR outputs are shown in Table I. It includes all paths which provide partial swing and full swing at the output nodes. For the input AB: "01," the transistors P2, N1, P4 turn on. Transistors P2 and N1 pass logic "1" and logic "0" at XOR and XNOR outputs, respectively, while transistor P4 turns in the transistor P3 to pass the weak logic "0" (-VTHP) at the output. Similarly, for the input AB: "10," transistors P1, N2 and N4 turn on. Transistors P1 and N2 pass logic "1" and logic"0" at XOR and XNOR outputs, respectively, and transistor N4 turns on the transistor N3 which passes the weak logic "1" (VDD-VTHN) at the XOR output. For these input (AB" "01" and "10"), the weak logic outputs will not affect the output swing as paths are available for full swing outputs.

For the input AB: "00," the transistors P1, P2, P4 and P5 turn on. P1 and P2 pass weak logic "0" (-VTHP) at the XOR output, while P5 and P4 pass full logic "1" at XNOR output and the terminal node X. Logic "1" at node X turns on the transistor N3 and a strong logic "0" is passed at the XOR output to make the full swing. Similarly, for input AB: "11," transistors N1, N2, N4 and N5 turn on. The transistors N1 and N2 pass weak logic "1" (VDD-VTHN) for the XNOR output, while the XOR node discharges completely through N4 and N5. Logic "0" also passes to the internal node X, which causes transistor P3 to be turned on and passes the full logic "1" at the XNOR output.

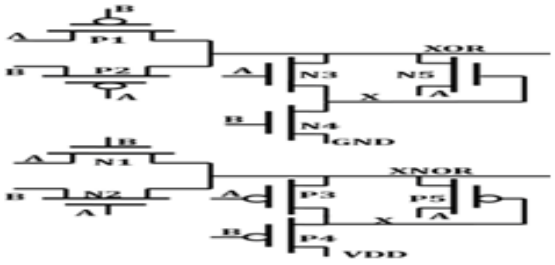

Fig.4. Proposed XOR-XNOR circuit for Full Subtractor

An XOR-XNOR circuit proposed by Radhakrishnan provides full swing outputs uses only six transistors. This configuration is realized using the CPL logic and feedback restorer transistors. It provides good performance for the inputs AB: "01" and "10" . However the switching delay arises at the output for the input

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AB:"11" and "00". The issues of higher delay for these inputs is resolved by the method using by Naseri and Timarchi by adding 2nmos and 2pmos transistors. The proposed XOR-XNOR gate is symmetrical and NOT logic has been incorporated into it without using external NOT gate. Due to this incorporated NOT gate , the capacitance equivalent to one inverter at the input node is reduced which reduces the overall delay. The output nodes of the circuit are charged and discharged through different full swing and partial swing paths for different input combinations. The delay for an input combination can be decreased by reducing the sizes of transistors along its path. However, increasing the size of the transistor increases the capacitive load at the node, which increases the delay for the other input combinations.

III. FULL SUBTRACTOR CIRCUIT DIAGRAM

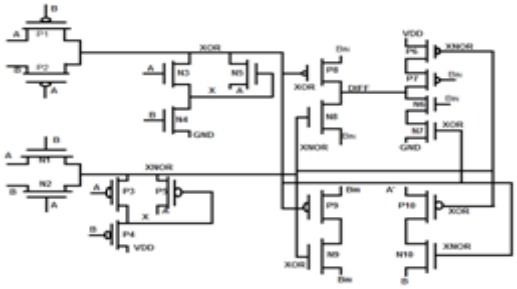

Fig.5. Full Subtractor circuit diagram

In this design FS cell module 2 and module 3 are implemented using CMOS logic style as shown in the figure. This circuit gives the best performance in terms of delay and PDP. This FS circuit 22 transistors for generating the DIFF and BOUT. Full Subtractor is one of the most used and essential combinational logic circuits. It is a basic electronic device, used to perform subtraction of two binary numbers. The Full Subtractor uses binary digits like 0, 1 for the subtraction. The circuit can be built with logic gates such as OR, XOR, NAND gates. The inputs of this subtractor are A, B, BIN and outputs are DIFF, BOUT.

Table II: Performance comparison of XOR-XNOR circuit in terms of power dissipation, delay, and PDP

XOR-XNOR Circuits	No. of Transistors	Delay (ps)		Power (μW)	PDP (10^{-18})
		XOR	XNOR		
Aguirre [6]	12	59.6	58.9	8.01	479.79
Goel [3]	8	140.9	141.8	10.37	1470.46
Radhakrishnan [13]	6	106	96.5	10.9	1144.4
Chang [4]	10	98.8	70.8	10.8	1057.16
Valshani [14], [17]	10	73.7	52.2	10.7	788.59
Naseri [15]	12	52.9	49	8.98	475.04
Proposed	10	48.3	49.4	8.89	439.16

Performance of the proposed XOR-XNOR circuit is compared with the existing circuits in terms of worst case delay, power consumption, and PDP in Table II. The delay is calculated from the 50% voltage level at the input to 50% voltage level at the output for all the rise and fall transition, and worst case delay is selected. For the calculation of PDP, the worst case delay of XOR and XNOR outputs is taken. The XOR-XNOR circuit, presented in [13] uses the least number of transistors. However, it has a high worst case delay. In [6], two XOR-XNOR circuits are presented in which the design which has least PDP is included in the table for comparison. The proposed XOR-XNOR circuit has the least worst case delay among all the designs. In terms of power consumption, the design presented in [6] gives the best performance. However, the PDP of the proposed circuit is least among all the circuits. The proposed XOR-XNOR circuit shows improvement in terms of delay and PDP up to 65.16% and 70.13%, respectively, than those of other designs.

IV. POWER CALCULATIONS

A comparison of the proposed arithmetic design with other arithmetic designs in terms of the number of transistors, delay, power consumption, and PDP is considered from the reference. For the calculation of the delay, DIFF to Bout delay is considered as this delay is crucial for most of the high level designs. In H.Naseri, six designs of FA_s are presented. The proposed design provides best delay performance among all the designs, and the proposed design have the lest PDP compared to other designs.

V. FULL SUBTRACTOR CIRCUIT GENERATED IN THE TANNER TOOL

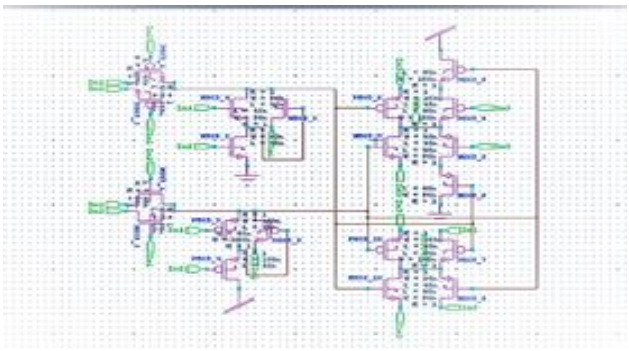

Fig.6. Proposed Full Subtractor circuit

For the execution of the circuit, the software used is TANNER TOOL. Tanner tool is a software suite for the design, layout and verification of analog, mixed-signal, RF and MEMS ICs. It is an efficient platform from design capture through verification.

5.1. Input

The input to the proposed circuit is given as 111, 110, 101, 100, 011, 010, 001, 000 . As there are three inputs A, B, C, the below figure represents waveform for each inputs. Based on the inputs we gives the required output is generated.

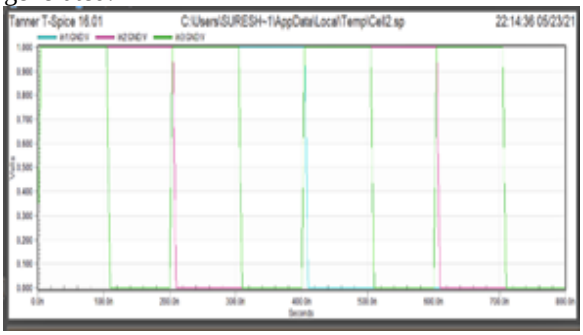

Fig.7. Input for the Full Subtractor

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5.2. Output

The outputs for the Full Subtractor circuit are shown in the below figure.

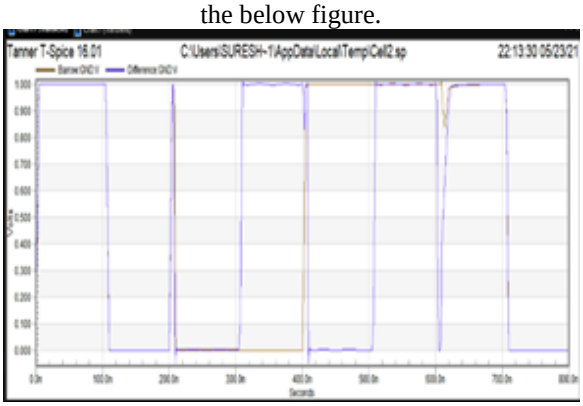

Fig.8. Output for the Full Subtractor

VI. CONCLUSION

The main advantage of the hybrid style is that all the modules can be optimized at the individual level and the number of transistors can be reduced which can reduce the internal power dissipation. The proposed circuit provides full swing output simultaneously. The inputs are in the digital form, for the different inputs like 111, 110, 101, 100, 0111, 010, 110, 000 the outputs generates are 11, 00, 00, 10, 01, 11, 11, 00 which are the digital outputs. The performance of the proposed circuit can be simulated by using tanner tool software.

REFERENCES

[1] Jyoti Kandpal, Abhishek Tomar , Mayur Agrawal and K. K. Sharma, "High Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR-XNOR Cell", IEEE Trans. Very large scale integration (VLSI), Vol.28,pp.1413-1422,April,2020

[2] P. Chandrakasan, S. Sheng, and R. W. Brodersen, “Low-power CMOS digital design,” IEICE Trans. Electron., vol. 75, no. 4, pp. 371–382, 1992

[3] R. Zimmermann and W. Fichtner, “Low-power logic styles: CMOS versus pass-transistor logic,” IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[4] S. Goel, A. Kumar, and M. A. Bayoumi, “Design of robust, energy efficient full adders for deep- submicrometer design using hybrid-CMOS logic style,” IEEE Trans. Very Large Scale Integer. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[5] C.-H. Chang, J. Gu, and M. Zhang, “A review of 0.18-µm full adder performances for tree structured arithmetic circuits,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.

[6] N. Zhuang and H. Wu, “A new design of the CMOS full adder,” IEEE J. Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.

[7] M. Aguirre-Hernandez and M. Linares-Aranda, “CMOS full-adders for energy-efficient arithmetic applications,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 718–721, Apr.2011.