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DESIGN AND SIMULATION OF DIGITALLY CONTROLLED OSCILLATOR OF ADPLL

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Abstract: In biomedical implants, the RF transceivers require the low power and less size components for acquiring best results in frequency and phase controlling. The RF transceivers obtain the information from either sides of sources in biomedical applications. Access the signal from human body and processed it through amplifiers, Phase Locked Loops (PLLs), mixers & filters and many more for controlling the parameters. Majorly the PPLs provide the required frequency for the entire operation to obtain this All Digital Phase Locked Loop (ADPLL) is mostly used. In ADPLL, DCO is a major block through which fine frequency resolution is achieved. The present project concentrates on designing the low power Digitally Controlled Oscillator (DCO).

Keywords: PLL, ADPLL, DCO, Low Power, Frequency tuning.

I.INTRODUCTION

Currently in high performance systems All-Digital Phase Locked Loops (ADPLLs) are used. With the utilization of ADPLLs in digital communication systems, the use of digitally controlled oscillators (DCO) over voltage controlled oscillators (VCO) has come into existence. The general block diagram of ADPLL is shown in figure 1. In general ADPLLs the phase detector generates an output (v_d) phase/frequency signal by consideration of difference between the input (v_1) and signals from DCO/Digital VCO (v_2'). Later "v_d" undergoes through a filter and responsed as "v_f" this once again linked with DCO and generated as "v_2'". This controlled closed loop function will continue till the end of the process. In this scenario DCO has a crucial role.

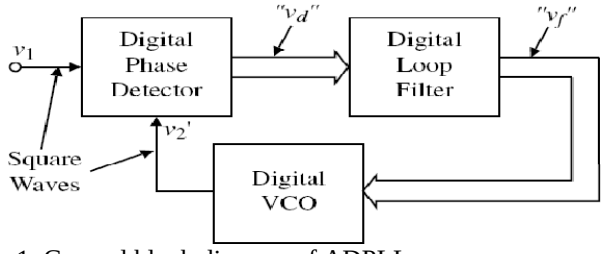

Fig.1. General block diagram of ADPLL

Hence a low voltage and low power digitally controlled oscillator (DCO) utilized in a medical implant communication service (MICS) frequency band designing is the aim of this paper. In this paper, a new low power DCO structure is proposed with NMOS delay cells as switching network.

II. DCO

Due to the development of technologies like nano, femto, IOTs the usage of digital components or ADPLLs in various interactive devices proposes the DCO. This paper concentrates on DCOs evolution in modern electronic devices as well as their performances in local oscillators. Research is still continuing on DCOs to get best performance in device area, fastness, range of frequency, power dissipation, low supply voltages etc. The aim is to understand and track the advances in DCO based on its performance level.

DCO is an oscillator circuit that produces simple flag whose recurrence is constrained by advanced information. Be that as it may, in the event of VCO, recurrence is set by the control voltage. The following diagram shows the basic block diagram of DCO.

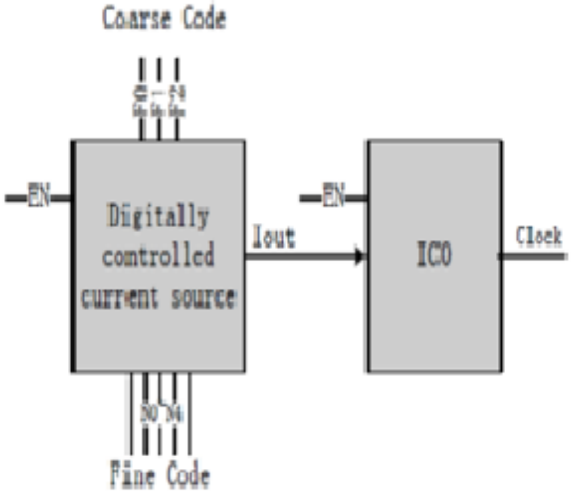

Fig .2.Basic Block Diagram of DCO

The functional block diagram of DCO circuit is shown in Fig. It is composed of current controlled oscillator and digitally controlled current source. F0~F1 is the Coarse Code of tuning output current from the digitally controlled current (DCO) source, while N0~N4 is a Fine Code. The controlled bits F0~F1 and N0~N4 influences the value of output current so as to determine the frequency of the output clock signal from the current controlled oscillator.

2.1 Overview of DCO:

Digitally Controlled Oscillator (DCO) was planned with the goal that the oscillator is controlled carefully. For the control of recurrence scope of oscillator utilizing an advanced escalated approach, computerized control words in paired bits are bolstered into the oscillator. These

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advanced control words are coordinated in a DCO center that controls the recurrence scope of oscillator.

2.2 Types of DCO:

The different types of DCOs are:

1. Divide by N counter
2. Increment/Decrement counter
3. Bootstrapped DCO
4. XNOR DCO
5. LC DCO

Table I: Comparison of DCO

S.No.	DCO		
	Types	**Advantages**	***Disadvantages***
1	Divide by N counter	Lucid architecture [2]	No Jitter design concept [2]
2	Increment – Decrement Counter	Mastery over Hold & Lock range [1]	Software implementation is not possible [1]
3	Bootstrapped DCO	High linearity & resolution [3]	Heavy architecture [3]
4	XNOR DCO	*Direct path between VDD and GND is eliminated through optimized XNOR gate. Power Dissipation reduced [present work]*	*Because of the resistance of switch network the circuit delay is increased [present work]*
5	Differential LCDCO	*Good at low voltage operations*	*Introduce noise at high frequency ranges*

2.3 Performance of DCO:

The advancement of DCO execution depends on CMOS scaling, supply voltage, goals, control utilization and recurrence tuning range. The execution development for every parameter base on proposed examines is portrayed beneath.

2.3.1 Technology scaling:

Downsizing of CMOS components has been the driving force for DCO evolution. The CMOS technology development has been advanced with the downscaling of component size since the replacement of vacuum tubes with transistors few decades ago. This advanced technology process which leads to deep-sub micrometer CMOS benefits a lot to the circuit characteristics. Now, we are able to integrate millions of CMOS transistors in nano-scale in a silicon chip with few centimetres square. As the technology advances, the latest microprocessor operates at 3 GHz and is expected to increase further as well as RF communication devices.

2.3.2 Supply voltage in DCO implementation

Supply voltage is the most imperative explanation behind the replacing of VCO with DCO. Supply voltage is the working voltage for any type of oscillator. At the point when the CMOS downscaling was brought into the electronic field, the supply voltage likewise should have been decreased. Decrease of supply voltage in a simple circuit causes breakdown and unwavering quality issues. In this manner, the supply voltage must be little so as to accomplish an elite dimension. ADPLL utilizes the cell-based planned approaches other than LC or RC based, so it very well may be effectively incorporated into the computerized framework.

2.4 Power consumption in DCO implementation:

Power utilization of DCO ought to be decreased to spare by and large power dissemination to fulfill low power needs in SoC structures. ADPLL has a noteworthy inconvenience of extensive power utilization and 50 % of all out power is contributed by DCO. Power utilization is critical in convenient battery worked gadgets. Therefore, control sparing has turned out to be significant structure worry in current electronic gadgets. As the time passes, the power utilization has been diminished by improving the circuit plan. Low power prerequisites keep on being requesting for purchaser and different distinctive applications. All DCOs in PLLs being made today require a cost touchy power mindful vitality productive structure that can empower better frameworks. Building up the CMOS innovation and configuration to help exceptionally low power tasks is trying because of expanding gadget varieties and irregular changes. Along these lines, we depend on the improvement of innovation, yet need to search for novel circuit procedures and circuit topologies.

III. RESULTS AND DISCUSSION

DCO designed in this paper using XNOR based inverter with NMOS delay cells, which were connected in ring topology. Constructed and simulated using Tanner tools in 150nm technology. The operation of the circuit is as follows: the DCO shown in figure 3 with 3 delay cells with 3 control bits consists of a switch network with 4 NMOS transistors. These transistors are binary weighted with the first NMOS gate terminal connected to VDD supply for the provision of current conduction. The control bits D_0, D_1 & D_2 connected to remaining 3 NMOS transistors. The bit requirement decides by the frequency tuning range.

The extension may also possible for the proposed circuit, may implement using either 4 or 6 bit control DCO. But limited to 6-bit DCO due to circuit complexity issues. The control bits in 4-bit DCO (D_0 to D_3) and in 6-bit DCO (D_0 to D_5) are connect to weighted NMOS transistors.

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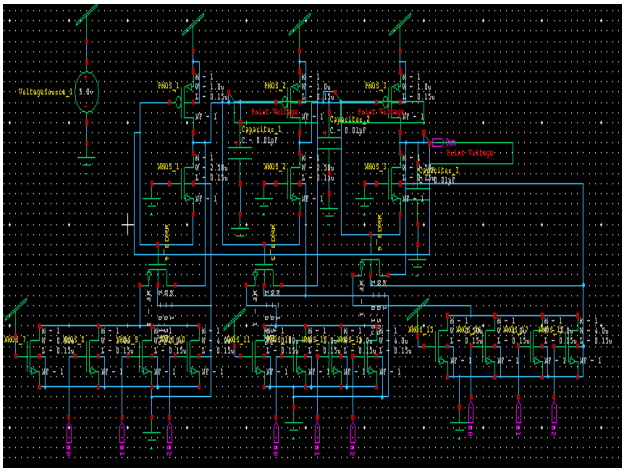
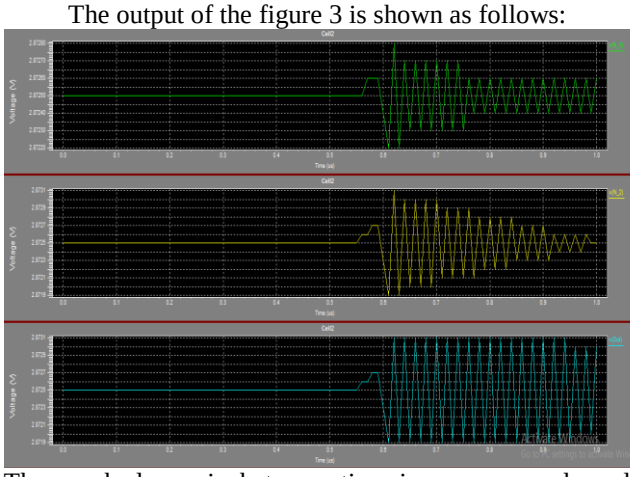


Fig.3.Schematic of DCO

The output of the figure 3 is shown as follows:



The graph drawn in between time in nano seconds and voltage in Volts, the first part in the waveform is obtained after the first stage of DCO circuit which provides less range of frequency ranges [1.3 to 1.67 GHZ]. The second obtained after the second stage which gives the moderate frequency range [1.25 to 1.67 GHZ]. The next one is at the output stage of proposed DCO which gives the best range of frequency for bio-medical applications [1 to 1.6 GHZ]. The power consumption for the proposed DCO structure, minimum power consumption is 6.813005e-003W at time 6.2e-007 Sec, the maximum power consumption is 6.817266e-003W at time 6.1e-007 SEC and the average power consumed for all combination of bits in DCO is 6.815116e-003W.

Table II: Comparison with previous circuits

DCO architecture	**Power dissipation in mW**	**O/P frequency in GHz**	**Technology (µm)**
Ref [4]	63.4	.333-1.47	0.35
Ref [5]	5.4	0.08-0.25	0.18
Ref [6]	25	1.2	0.6
Present work NMOS DCO	***6.8****	***1.0 -1.6***	***0.15***

CONCLUSION

The new structure for DCO using delay cells with control bits have been proposed in the present paper. The resistance nature of the circuit varies with respect to digital control bits and delay has been modulated. Due to an optimized circuit the power consumption of the proposed circuit is reduced noticeable. The DCO provides the output frequency range 1.0 to 1.6 GHZ with a power consumption of 6.8mWatts. The earlier reported details comparison table in terms of power dissipation, frequency ranges and technology used for design also presented in this paper. Based on the comparison table it is proved that the proposed circuit provides wide range of frequency with low power consumption.

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