SMERTMR: A Scan chain Multiple Error Recovery Technique for TMR System

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Abstract— In this paper a scan chain based multiple error recovery triple modular redundancy system is presenting to detect and recover the faulty module with the single or multiple errors in the modules. These errors are detected at the module's outputs where the proposed technique detects both multiple transient and permanent errors by using the scan chainflip-flops. If the transient errors were detected those are detected by comparing the internal state of the TMR module. Where detection of any mismatch between modules which are faulty modules was located and the states of fault free modules are copied in to the faulty modules. In case a permanent error is detected the system is updated to master/checker mode by disregarding the erroneous module. This system is designed and implemented by using Verilog HDL coding Xilinx 14.7 tool kit.

Index Terms— Triple Modular Redundancy (TMR), Scan chain Triple Modular Redundancy (ScTMR), Scan chain based Multiple Error Recovery Triple Modular Redundancy (SMERTMR), latent faults, permanent faults, Real time computing.

I.INTRODUCTION

A lot of research is going now a days in VLSI design domain to make designs more reliable and error resistant, For all the critical applications, we need to develop techniques which will make a design more reliable and error resistant. Simply testing and check isn't sufficient to build the unwavering quality of the system but configuration should have inbuilt property to tolerate the fault, if any happens while the device is in activity. Additionally, simply fault tolerance is not sufficient without joining the fault recovery methods likewise inside the outline. In the event that the ALU itself got faulty, the whole device will come to end [1].

Fault tolerance basically means guaranteeing the correct operation despite a fault occurrence, and thus signifies higher reliability. The fault occurring internally or externally is said to be masked or successfully hidden from being observed by the outside world. On the contrary, if the fault is not masked, it would affect the desired output expected from a function module causing an erroneous output to be produced instead of producing the correct output. Intermittent faults refer to those which are activated during certain times and are deactivated during other times, i.e. they occur randomly and might become permanent, for example, a loose electrical connection. Permanent faults are generally modeled using stuck-at faults There are two kinds of stuck- at faults viz. stuck-at-1 (abbreviated as, s-a-1) and stuck-at-0 (abbreviated as, s-a-0). There are two kinds of stuck-at faults: 1.Single stuck-at fault 2.Multiple stuck-at faults. Single stuck-at fault presumes that a function module contains only one fault. The multiple stuck-at faults model acknowledges that two or more faults can occur at the same time in a function module. Moreover, the multiple stuck-at faults is classified as unidirectional and bidirectional: unidirectional, if all the stuck-at faults are of the same kind (i.e. s-a-0 or s-a-1); and bidirectional, if the stuck-at faults are different (i.e. s-a-0 and s-a-1) [4]. A roll-forward recovery technique for TMR-based systems has been proposed in this technique, however, is not applicable for general-purpose circuits such as processors, as it requires detailed information about the function of all registers of TMR modules. A TMR-based technique applicable to general-purpose circuits has been proposed in this. The proposed technique, called ScTMR, provides recovery for both transient and permanent errors in TMR systems. ScTMR uses a roll-forward approach and utilizing in the scan chain implemented in the circuits for testability purposes to recover the system fault-free state [8].

First, ScTMR can't recover a single faulty module in the TMR system in the presence of latent faults. A fault is referred to as latent if it isn't propagated to the system outputs but can cause a mismatch between the states of the TMR modules. Second, ScTMR is unable to recover the system if multiple faults are simultaneously manifested to the outputs of two modules. Once a transient error is detected, the states of one of the fault-free modules are coping to the faulty module utilizing the scan chains. As no recomputation is needed, ScTMR has lower performance overhead compared to rollback recovery techniques. In case of permanent faults, the faulty module is disregarded and the system will be corrupted to the master/checker (M/C) configuration [9]. The Scan chain based Multiple Error Recovery TMR has the capability to identify and restore latent faults in TMR modules and also restore the system from multiple faults affecting two TMR modules. It compares the internal states of TMR modules to identify and restore the error-free state using the state of non-faulty modules. In case of permanent faults the system is updated to a master/checker (M/C) configuration. In roll-forward recovery mechanisms there is no recomputation as compared to retry based recovery mechanism hence it can be used in safety critical applications [6].

II. LITERATURE SURVEY

A. DESIGN APPROACH FOR FAULT TOLERANCE IN FPGA ARCHITECTURE.

Ms. Shweta S et al. [1] Failures of nano-metric technologies owing to defects and shrinking process tolerances give rise to significant challenges for IC testing. In recent years the application space of reconfigurable devices has grown to include many platforms with a strong need for fault tolerance. While these systems frequently contain hardware redundancy to allow for continued operation in the presence of operational faults, the need to recover faulty hardware and return it to full functionality

quickly and efficiently is great. In addition to providing functional density, FPGAs provide a level of fault tolerance generally not found in mask-programmable devices by including the capability to reconfigure around operational faults in the field. Reliability and process variability are serious issues for FPGAs in the future. With advancement in process technology, In regular structure like FPGA, redundancy is commonly used for fault tolerance. In this work we present a solution in which configuration bit-stream of FPGA is modified by a hardware controller that is present on the chip itself.

B. SCTMR: A SCAN CHAIN-BASED ERROR RECOVERY TECHNIQUE FOR TMR SYSTEMS IN SAFETY-CRITICAL APPLICATIONS.

Mojtaba Ebrahimi Seyed [2] They propose a roll-forward error recovery technique based on multiple scan chains for TMR systems, called Scan chained TMR (ScTMR). ScTMR reuses the scan chain flip-flops employed for testability purposes to restore the correct state of a TMR system in the presence of transient or permanent errors. In the proposed ScTMR technique, we present a voter circuitry to locate the faulty module and a controller circuitry to restore the system to the fault-free state. As a case study, we have implemented the proposed ScTMR technique on an embedded processor, suited for safety-critical applications. Exhaustive fault injection experiments reveal that the proposed architecture has the error detection and recovery coverage of 100% with respect to Single Event Upset (SEU) while imposing a negligible area and performance overhead as compared to traditional TMR-based techniques.

C. IMPLEMENTATION OF ERROR RECOVERY IN TMR SYSTEMS USING SCAN CHAIN-BASED TECHNIQUE.

Sarfaraz Nawaz Qureshi et al.[3] In this project a scan chain based technique is employed to recover multiple errors in Triple modular redundancy (TMR) systems. This technique can detect both permanent faults and transient faults (temporary faults) and can be used in safety critical applications such as patient care systems, avionics, etc. Real-time computing systems are extensively used in our daily lives. On detection of any mismatch, the faulty or erroneous modules are identified and the state of an error free module is copied into the erroneous modules. In case a permanent fault is detected, the system is updated to a master/checker mode by disregarding the erroneous module. Exhaustive fault injection experiments reveal that the this architecture has the maximum error detection and their recovery and imposes a negligible performance and area overhead as compared to traditional techniques based on TMR.

III. RELATED WORK

In this paper the two important methods are discussed which are useful for this paper and these techniques are used in this paper

1. TMR Technique.
2. ScTMR Technique.

The TMR technique

We can enhance the reliability of any digitalized system by properly using redundant designs. In majority of the cases faults occur at the hardware level, so we prefer using triple modular redundancy in order to diminish the chances of hardware failure [4]. Triple modular redundancy is the most common type of redundancy method which has been discussed further in this paper. Triple Modular Redundancy, (TMR) is a fault-tolerant structure of N-modular redundancy, in which three systems execute a procedure and that outcome is prepared by a voting system to design a single output. The main logic behind the use of triple modular redundancy is that, all the important systems are triplicates and regardless of whether any of one out of the three flops then the remaining two operational units works hand in hand in order to correct the faulty output. The voting logic evaluates the output of all the modules and then it passes the majority output i.e. if all three outputs are equal then it turns out to be the final output and if two out of three outputs are equal then the two similar outputs turn out to be the final output. Also, if the two equal outputs are falsified output then it will turn out to be the final output [8].

The ScTMR technique

TMR is an important and widely used fault tolerant technique. It can select the correct output in the presence of a faulty module, but unable to detect and correct the faulty module. Also it fails if multiple modules are faulty and if he voter is faulty. If an error occurred in a module is not corrected, then in the next cycle of operation another module may become faulty and thus it leads to the problem of multiple faulty modules. All error recovery techniques should have the ability to rewrite the faulty module with the state of fault free module on the detection of an error [5]. The ScTMR technique reuses scan chains for recovering the condition of the faulty module. Scan chain is a cost effective technique used in Design for Testability (DFT) to provide a basic method to testing combinational and sequential circuits. In this technique, flip-flops are chained together through a long shift register circuit and a multiplexer is used as part of front of each flip-flop to switch between the normal and testing operations. In order to reduce the observation and loading time in large designs multiple scan chains are used. Multiple scan chains include parallel chains, which consist of approximately the same number of flip-flops. The number of flip-flops in each scan chain is called scan chain length (Lsc) and the number of scan chains in parallel is named scan chain width (Wsc) [9].

Fig .2 shows the block diagram of the ScTMR technique. As shown in this figure, the ScTMR includes: 1) three redundant modules; 2) a voter; and 3) a controller. In this architecture, once an error is detected by the voter, the ScTMR controller identifies the error type (transient or permanent) and triggers an appropriate recovery mechanism to remove the error from the system. This is achieved by copying the state of a fault free module to the detected faulty module using the scan-chain circuitry. The recovery process is done by the scan-chain input (SCI),

scan-chain output (SCO), and scan-chain enable (SCE) signals introduced by the ScTMR controller [8].

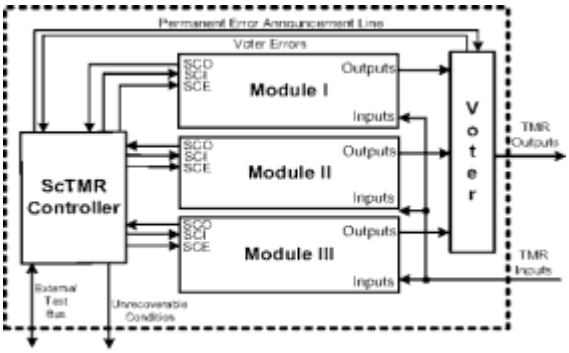

Fig 1. ScTMR block diagram [8].

IV. PROPOSED TECHNIQUE

Proposed voter circuit

In a TMR system, detection and correction of a faulty module is a challenging issue and is still an ongoing research topic. In particular, a wrong detection or inability to locate the faulty module can significantly affect the system reliability. To solve this issue, a voter that can identify the faulty module is presented. Additionally, the proposed voter can also identify the possible faults occurring in the comparators [3]. The proposed voter can be utilized in both ScTMR and SMERTMR techniques [7].

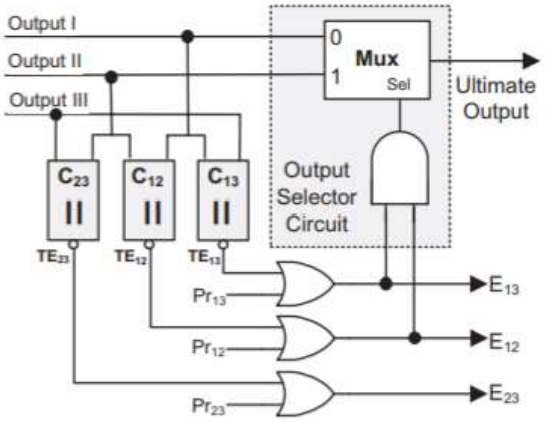

Fig 2. Voter circuit [7].

The architecture of the proposed voter is shown in Fig 1. As shown in the figure, three comparators (C12, C13, and C23) are used to represent any mismatch between TMR modules. As an example, E23 signal is activated once a mismatch between Outputs II and III is detected. If one of these modules generates an erroneous output (e.g., Output I), two of the comparators (here, C12 and C13) will activate the mismatch signals (here, E12 andE13) and only one of the comparators (here, C23) will not activate the corresponding mismatch signal (here, E23). In this case of a faulty comparator (e.g., C13), only the corresponding signal (here, E13) is activated and the other signals (here, E12 and E23) are deactivated. In order to detect permanent faults, the proposed voter employs three input signals (named Pr12, Pr13, and Pr23), which are derived by the ScTMR controller. In the normal state and during transient error recovery process, these three signals are deactivated (Pr12 = Pr13 = Pr23 = 0). In the proposed voter, an output selector circuit is used to route the error-free output to the ultimate output signal. As shown in Fig 1, the output selector circuit uses E12 and E13 signals as inputs of a logical AND gate to generate the select signal for a 2×1 multiplexer [3]. The value of error signals shown in Table 1 identifies the faulty module or faulty component and selects the correct voter output. For instance, if E12 E13 E23 =101, module II is identified as the faulty module and Output I is selected as an error-free output [7].

Table 1: Identifying faulty module and selecting correct voter output using error signals.

E_{12}	E_{13}	E_{23}	Faulty module	Output
0	0	0	–	Output I
0	0	1	C_{23}	Output I
0	1	0	C_{13}	Output I
0	1	1	Module III	Output I
1	0	0	C_{12}	Output I
1	0	1	Module II	Output I
1	1	0	Module I	Output II
1	1	1	Unrecoverable	X

Briefly, according to Table 1, if one of the comparators, module II, or module III becomes faulty, the output of module I is selected as the error-free output. If module I become faulty, output II will be selected as the error-free output. Based on this specification, the output selector can be implemented by a 2 × 1 multiplexer. In the new voter proposed error signals will be generated in case of difference between the module outputs. These error signals will trigger the controller to correct the module outputs and thus produce accurate output [8].

In this paper the SMERTMR technique has been proposed for recovering multiple errors up to two errors and it is called as scan chain based multiple error recovery technique for TMR systems (SMERTMR). This technique operates in two modes: Comparison mode and recovery mode. The comparison mode is activated in the following two cases: First when the voter detects an error and second when the checkpoint signal is asserted. In the second case, the checkpoint signal is utilized to trigger the comparison mode so that latent faults can be eliminated. The comparison mode can be activated once an error in a module propagates to the outputs of the module and voter detects it. So when the comparison mode isn't frequently activated by the checkpoint signal, latent faults are detected and identified once a next fault is propagated to the module outputs and detected by the voter. In the SMERTMR technique, the comparison mode is activated when an error is detected by the voter [4].

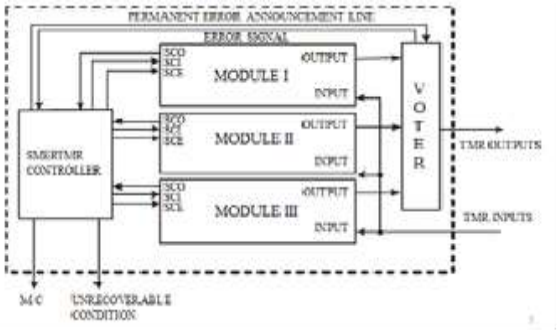

Fig3. Block Diagram of SMERTMR [7].

As mention earlier, in the SMERTMR technique the internal states of TMR modules are compared together, while in the ScTMR technique only the module outputs are compared by the voter In the comparison mode, the internal states of the TMR modules are compared with each other to locate faulty modules and to determine the fault type. If no mismatch is found between all comparison pairs of the modules, the system returns to its normal mode. Otherwise, the system switches to the recovery mode and the recovery process is started. Finally, if the recovery process finishes successfully, the system continues to operate in the normal mode. As a result of this following advantages are achieved for SMERTMR technique: 1) In case, if there is enough slack time to regularly execute the comparison process, the chances of having multiple faulty modules is significantly decremented. 2) 2 faulty modules can be efficiently detected and identified. So, the faulty modules can be recovered using the states of the fault-free or error-free module [6].

SMERTMR STATE DIAGRAM

In Fig 4.It shows the state diagram of SMERTMR. At first the system is in the ordinary state. Upon the recognition of an error by the voter, it enters in to the comparison mode. If no error is discovered, then it resets. If the error is single or multiple transient faults, then it enters into the recovery mode. If the single or multiple transient errors is recovered successfully, it resets to normal mode. Otherwise, it enters in to the unrecoverable condition. The system will halt here. If the fault is permanent, then the system is degraded into the master/checker configuration that ignores the state of the Triple Modular Redundancy modules. Both of the master or checker modules are faulty, and then the system goes into the unrecoverable condition. When the error is detected by the voter and the comparison process can't recognize faulty modules, then the system enters into the unrecoverable condition [7].

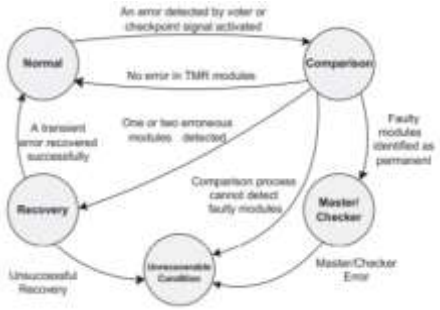

Fig 4. State diagram of SMERTMR [7].

COMPARISON PROCESS

In the SMERTMR technique, at whatever point the voter detects an error, it activates an error signal to alert the SMERTMR controller. Upon activation of the error signal, the SMERTMR controller switches from the normal operation to the comparison mode which locates the faulty modules. After finding the faulty modules, SMERTMR switches to the recovery mode to recover controller circuit working in the comparison mode [8]. In this mode, the internal states of all TMR modules are shifted out utilizing the scan chains and all module pairs (I/II, I/III, and II/III) are compared. In SMERTMR modules the SMERTMR controller enables the scan chains and configures the multiplexers in such a way that the SCO signal and SCI signal is connected in each module of the similar module. During the shift operation, the internal states of the modules are compared utilizing XOR gates. At whatever point a mismatch is recognized, the comparing counter is incremented by one unit. The Fault Locator Unit (FLU) recognizes the faulty module utilizing the faulty module recognition algorithm. The FLU stores the faulty module number in the Faulty Modules Register (FMR) [7].

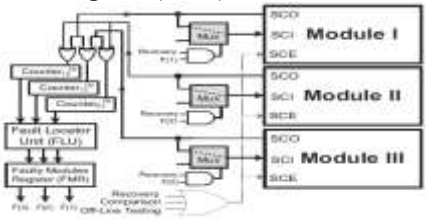

Fig 5.SMERTMR in comparison mode [4].

RECOVERY MODE

In the recovery mode, the faulty module is recovered by the state of fault free modules are utilizing the utilized scan chains. In SMERTMR module the SMERTMR controller enables the scan chains and configures the multiplexers as follows: The SCI signal of fault-free modules is connected to the SCO signal of the same module. Moreover, the SCI signal of the faulty module is connected with the SCO of one of the fault free modules; the value of the FMR register is used in the recovery mode to select the incoming driver of the appropriate signal driver for the SCI signals. The state of one of the fault-free modules is copied into the faulty modules after Lsc clock cycles [7].

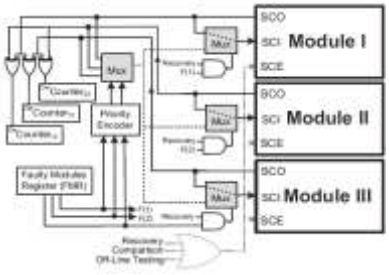

Fig 6. SMERTMR in recovery mode [7]

During the recovery process, at whatever point a mismatch is detected and the corresponding counter value containing the quantity of mismatches is decreased by one unit. Towards the finishing of this recovery process, all counters should be zero. This is because, for each mismatch, the relating counter is incremented by one unit

during the comparison process and is decremented by one unit during the recovery process. If either of the counters is nonzero towards finish of the recovery process, it is indicative of any other fault occurrence during the recovery process. In this case, the SMERTMR system would enter the unrecoverable condition since such faults cannot be located.

V.SIMULATION RESULTS

Simulation of ScTMR

The below simulation results depict the output of ScTMR technique. It can be seen that errors are injected in single module i.e. module I. Due to this output of this module vary and are erroneous. The system is able to detect error and it error recovers. Once the error is detected recovery mode is activated. Hence outputs of the erroneous module are restored to the fault free state.

Fig 7: Simulation result for AND operation of two variables using ScTMR.

In the above simulation results we are doing AND operation as in Fig 7. The input as 001110010 and input b as 01010000 are ANDed with each other the output is 00010000. In this simulation result module I is faulty and module II, module III are fault free. Once error detected then by using ScTMR technique and TMR technique the result will erroneous.

Simulation of SMERTMR

The below simulation results depict the output of SMERTMR technique. It can be seen that errors are injected in two modules i.e. module I and module III. Due to this outputs of these modules vary and are erroneous. The system is able to detect both of these errors as it supports multiple error recovery. Once the error is detected comparison mode is activated to detect the errors and consecutively the recovery mode is activated. Hence outputs of the erroneous modules are restored to the fault free state.

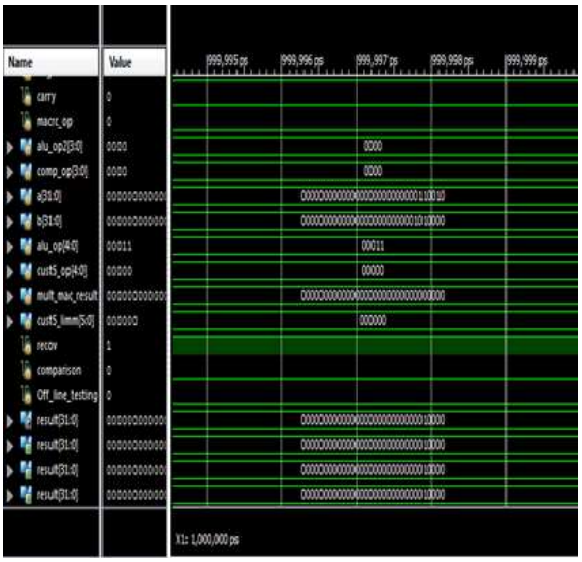

Fig 8: Simulation result of recovered modefor AND operation of two variables using SMERTMR.

Fig 9: Simulation result of unrecovered modefor AND operation of two variables using SMERTMR.

In the above simulations results we are showing recovered and unrecovered results by using SMERTMR technique. Here we are going to do AND operation using input a as 00110010 and input b as 01010000 both inputs are ANDed with each other the output is 00010000. Here in this module I and module III are faulty modules and module II is fault free module. Once error is detected in comparison mode it compares the inputs and recovery mode is activated i.e., recovery mode is high then the faulty modules are restored to the fault free state hence the output will be erroneous.

VI CONCLUSION

In this paper a technique called roll-forward technique is presented to recover errors using SMERTMR method in triple modular redundancy systems. The SMERTMR technique has the capability to recover multiple errors i.e. up to two faulty TMR modules. In this to be known that fault injection here is done manually. Inference can be

drawn that SMERTMR technique is quite reliable one as it is capable of countering more than one error. By using this SMERTMR technique we recover the modules internally of that system compared to ScTMR technique. The simulation of results is done in Xilinx 14.2 toolkit.

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