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COMPARATIVE STUDY OF THD REDUCTION FOR ASYMMETRICAL CASCADED H-BRIDGE INVERTER

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Abstract— This paper proposes the performance of single phase seven, thirteen and twenty seven level asymmetrical cascaded H-bridge multilevel inverter. This proposed inverter widely used in industrial applications such as speed control of induction motor, brushless dc motor etc. This paper reveals the reduction of total harmonic distortion when the number of levels gets increased. FFT analysis and output result of inverter is discussed in this paper.

Index Terms— Asymmetric, Multilevel inverter, THD, Voltage levels.

I.INTRODUCTION

Multilevel inverter is used to convert uncontrolled D.C to controlled A.C. In recent years, asymmetric multilevel inverters have received increasing attention because it is possible to synthesize voltage waveforms with reduced harmonic content, even using a few series- connected cells. In this paper seven, thirteen, twenty seven level inverter with it results has been discussed. For pulse generation sinusoidal pulse width modulation technique is used. This technique is most widely used in industrial application. FFT is used to determine the harmonic analysis for seven, thirteen and twenty seven level inverter.

Multilevel inverters include an array of power semi-conductors and dc voltage sources, the output of which generate voltages with stepped waveforms. In comparison with a two-level voltage-source inverter (VSI), the multilevel VSI enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference.

By increasing the number of levels in the multilevel inverters, the output voltages have more steps in generating a staircase waveform, which has a reduced harmonic distortion.

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II. PROPOSED SYSTEM

Multilevel inverter owns a separate DC source to form a single phase full bridge or H-bridge inverter. By different combination of four switches S1, S2, S3 and S4, it can generate the three different output voltage +Vdc, 0, -Vdc.

The switches S1 and S4 turned on to obtain a +Vdc, for –Vdc the switches S2 and S3 gets turn on. The output voltage is 0 when the switches S1 and S4 or S2 and S3 are turn on. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$V_{out} = V_{HB1} + V_{HB2} \qquad (1)$$

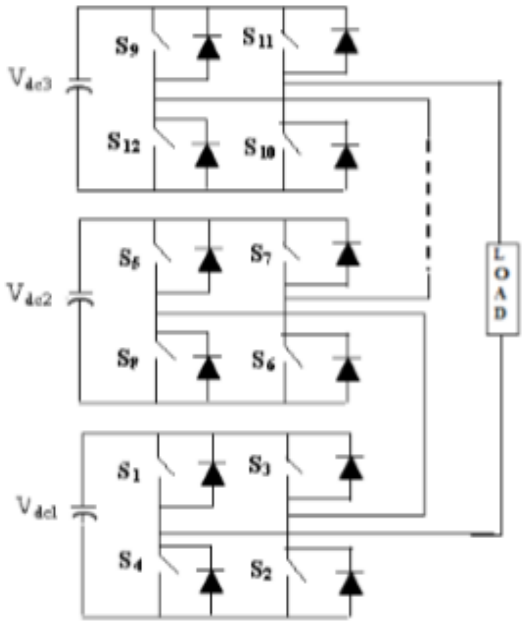

Figure 1: General Circuit for H-Bridge Inverter

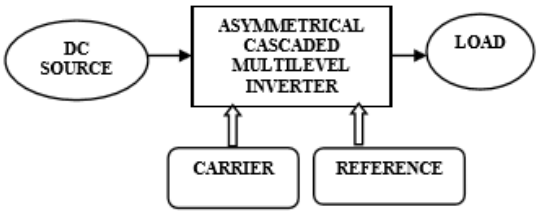

Figure 2: Block Diagram of Proposed syste

III. CIRCUIT DIAGRAM OF PROPOSED SYSTEM

Circuit diagram of Asymmetrical H-bridge multilevel inverter employing Binary DC input source shown in figure 3. By using Vdc, 2Vdc. it can synthesize seven output levels; 0, Vdc, 2Vdc, 3Vdc, -Vdc, -2Vdc, -3Vdc.

In the proposed circuit topology, if n is number of H-bridge module has independent DC sources in sequence of the power of 2 an expected output voltage level is given as $Vn = 2^n$, n = 1,2,3 (4)

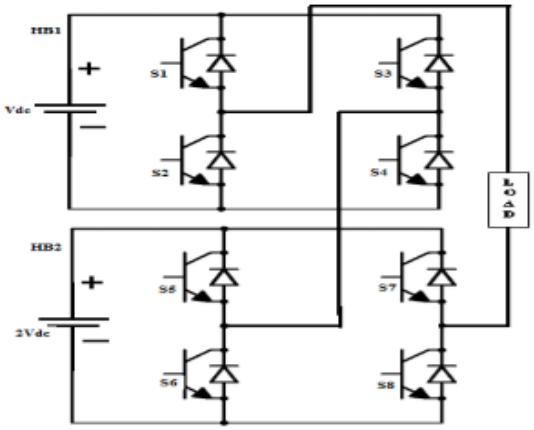

Figure 3: Circuit Diagram for Seven Level Inverter

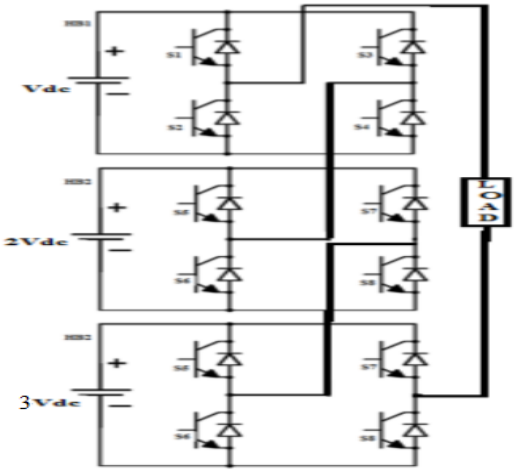

Figure 4: Circuit Diagram for Thirteen Level Inverter

Figure 4 shows the thirteen level inverter. It can synthesis fifteen output level 0, Vdc ,2Vdc , 3Vdc , 4Vdc , 5Vdc , 6Vdc , -Vdc , -2Vdc , -3Vdc , -4Vdc , -5Vdc ,6Vdc.

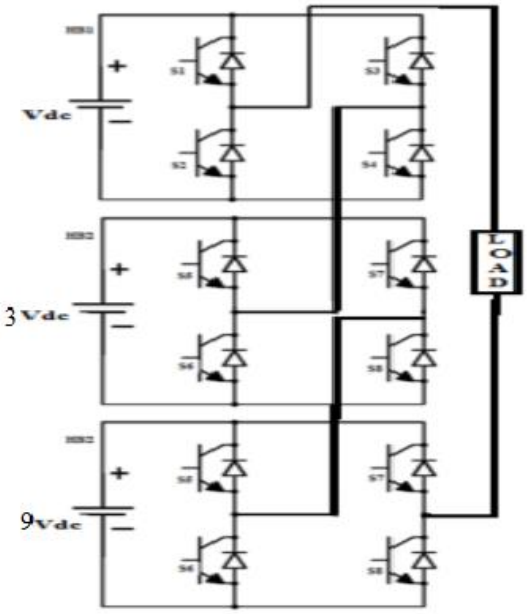

Figure 5: Circuit Diagram for Twenty Seven Level Inverter

Fig 5 shows the circuit diagram of twenty seven level inverter which is similar to the thirteen level circuit only difference is the value of dc voltages applied to each bridge. The ratio is 1:3:9 for twenty seven level inverter.

VI. SIMULATION RESULTS

The simulation model is done by using MATLAB / SIMULINK. The analyses of total harmonic distortion for proposed systems are given below:

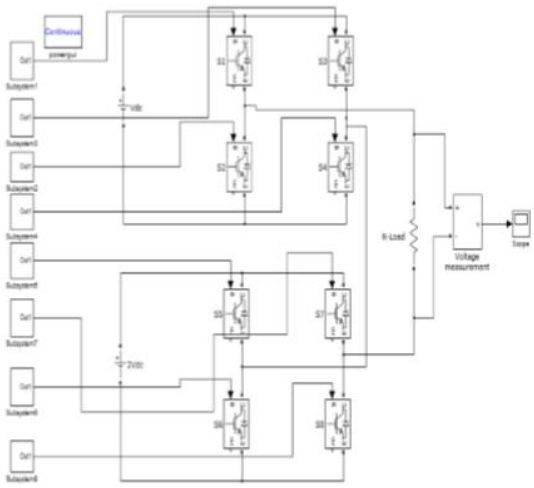

Figure 6: Simulation Circuit for Seven Level Inverter

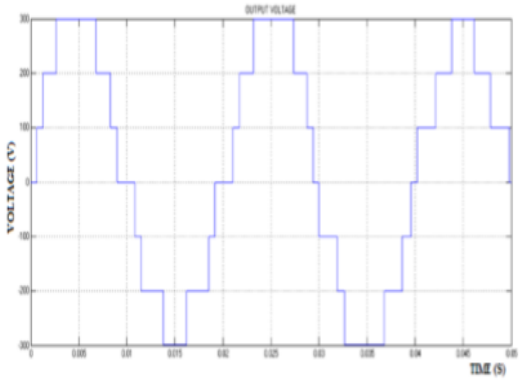

Figure 7: Output Voltage Waveform for Seven Level Inverter

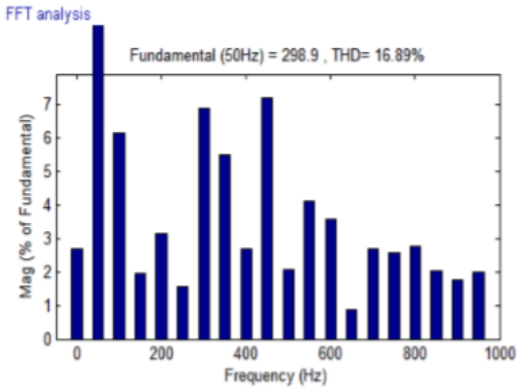

Figure 8: FFT for Seven Level Inverter

The figures 6,7 and 8 shows the simulation diagram, output voltage waveform and the FFT analysis for seven level inverter and the THD is obtained as 16.89%.

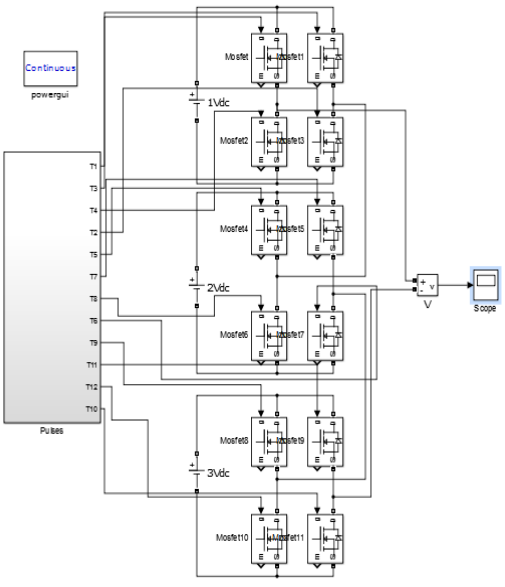

Figure 9: Simulation Circuit of Thirteen Level Inverter

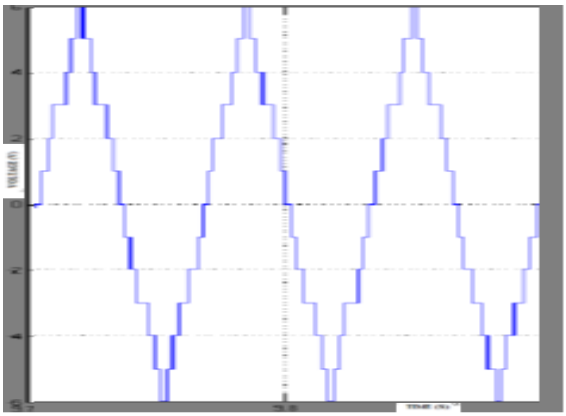

Figure 10: Output Voltage Waveform for Thirteen Level Inverter

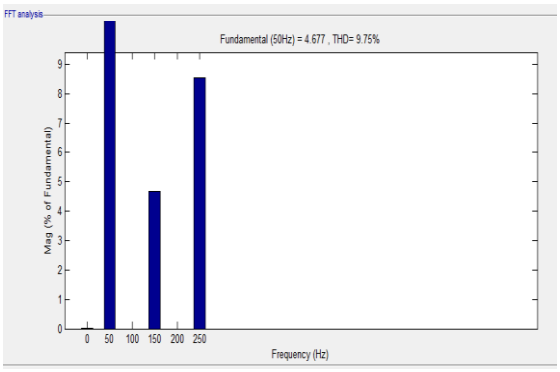

Figure 11: FFT for Thirteen Level Inverter

The figures 9,10 and 11 shows the simulation diagram, output voltage waveform and the FFT analysis for thirteen level inverter and the THD is obtained as 9.75%.

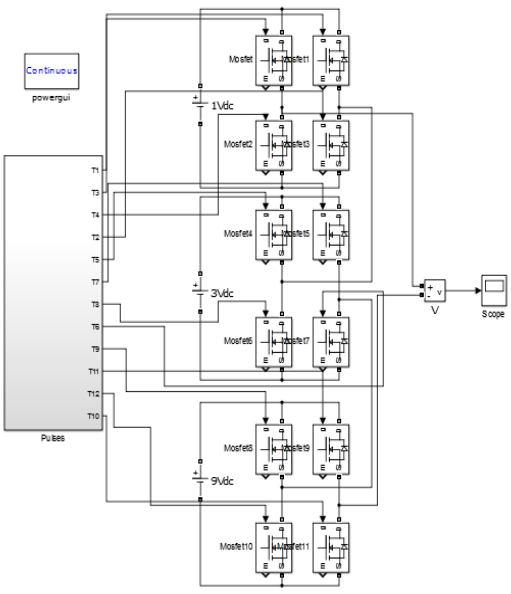

Figure 12:Simulation Circuit of Twenty Seven Level Inverter.

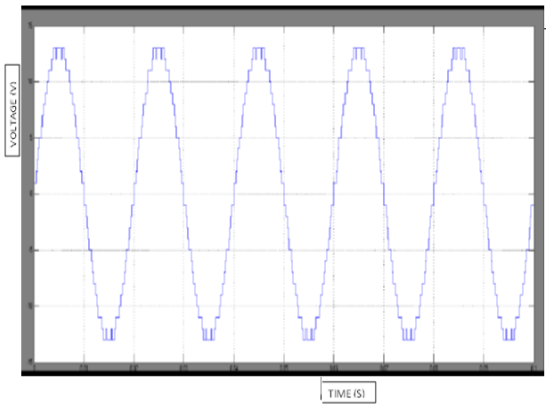

Figure 13:Output Voltage Waveform of Twenty Seven Level Inverter.

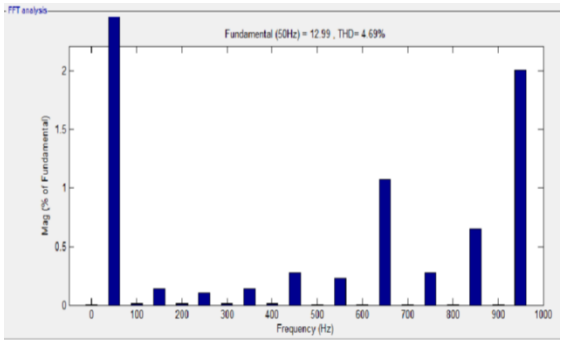

Figure 14:FFT analysis of Twenty Seven Level Inverter

Figures 12,13 and 14 level inverter shows the simulation diagram, output voltage waveform and FFT analysis for twenty seven level inverter and the THD is 4.69%.

V.COMPARATIVE ANALYSIS

S.NO	NO OF LEVELS	THD
1.	7 LEVEL	16.89%
2.	13 LEVEL	9.75%
3.	27 LEVEL	**4.69%**

Table 1: Comparative Analysis

From above comparative analysis, we can note that twenty seven level inverter has low total harmonic distortion compare to seven and thirteen level.

V. CONCLUSION

In proposed work, the performance of asymmetrical cascaded H-bridge seven level, thirteen level and twenty seven level inverter has been analysed by MATLAB / SIMULINK. From above comparative table, the twenty seven level inverter has **4.69%,** which has low total harmonic distortion compared to seven level and thirteen level inverter.

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