DESIGN AN PARALLEL PREFIX ADDER WITH SKIPPING OF LOGIC

GHERA SUVARNA RATNA
M.TECH – SCHOLAR – E.C.E
Dept. of E.C.E
MALINENI LAKSHMAIAH WOMENS ENGENERING COLLEGE
GUNTUR DT.

YENUGULA BHASKARA RAO
ASSOCIATE PROFESSOR
Dept. of E.C.E
MALINENI LAKSHMAIAH WOMENS ENGENERING COLLEGE
GUNTUR DT.

ABSTRACT: In this paper discussed about a carry skip adder (CSKA) structure with P.P.A compared with the conventional adder. A parallel-prefix adder gives the best performance in VLSI design. However, performance of P.P.A adder through black cell takes huge memory. So, gray cell can be replaced instead of black cell which gives the Efficiency in P.P. Adder. The three stages of operations in the proposed system are pre-processing stage, carry generation stage, post-processing stage. The pre-processing stage focuses on propagate and generate, carry generation stage focuses on carry skip generation and post-processing stage focuses on final result.
Index Terms—energy efficient, Carry Skip adder (CSKA), voltage scaling, hybrid variable latency adders, high performance.

I INTRODUCTION

Adders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. For optimizing the speed and power of these units there are many works, which have been reported. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors.

To lower the power consumption of digital circuits the effective technique used is, to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage.

In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic. The desire to have a reliably operating circuit under a wide range of supply voltages in highly scaled technologies is from the concentration on the static CMOS. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. To lower the power consumption without considerably impacting the CSKA speed, adjustment is done on the system which is based on the variable latency technique, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the super threshold region down to near-threshold region and also, it has been reported in the literature the design and structure of (hybrid) variable latency CSKA. Hence, the contributions of this paper can be summarized as follows.

1) To enhance the speed and energy efficiency of the adder a modified CSKA structure by combining the concatenation and the incrimination schemes to the conventional CSKA (Conv-CSKA) is proposed. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer.

2) For constructing an efficient CSKA structure a design strategy is provided based on analytically expressions presented for the critical path delay.

3) Investigating the impact of voltage scaling on the efficiency of the proposed CSKA structure (from the nominal supply voltage to the near-threshold voltage).

4) Based on the extension of the suggested CSKA a hybrid variable latency CSKA structure is proposed, by replacing some of the middle stages in its structure with PPA, which is modified in this paper.

II EXISTED SYSTEM

The existed hybrid variable latency CSKA structure is shown in Fig.1 wherein *Mp*-bit modified PPA is used for the *p*th stage (nucleus stage). Since the nucleus stage, which has the largest size (and delay) among the stages, is present in both SLP1 and SLP2, replacing it by the PPA reduces the delay of the longest off-critical paths. Thus, the use of the fast PPA helps increasing the available slack time in the variable latency structure. The input bits of the PPA block are used in the predictor block, so this block becomes parts of both SLP1 and SLP2.

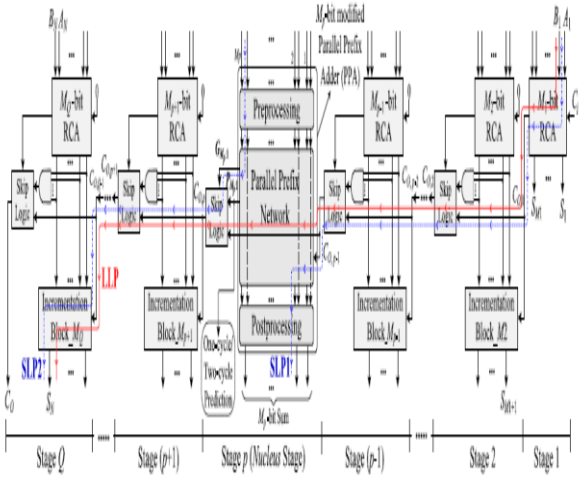


Fig.1 Structure of the Existed Hybrid Variable Latency

In the existed hybrid structure, the prefix network of the Brent–Kung adder is used for constructing the nucleus stage (Fig. 2). By using forward paths, the longest carry is calculated sooner compared with the intermediate carries, which are computed by backward paths is most important advantage of this adder when compared with other prefix adders .In addition, the fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. Finally, it has a simple and regular layout. The internal structure of the stage *p*, including the modified PPA and skip logic, is shown in Fig. 2. Note that, for this figure, the size of the PPA is assumed to be 8 (i.e., *Mp* = 8).

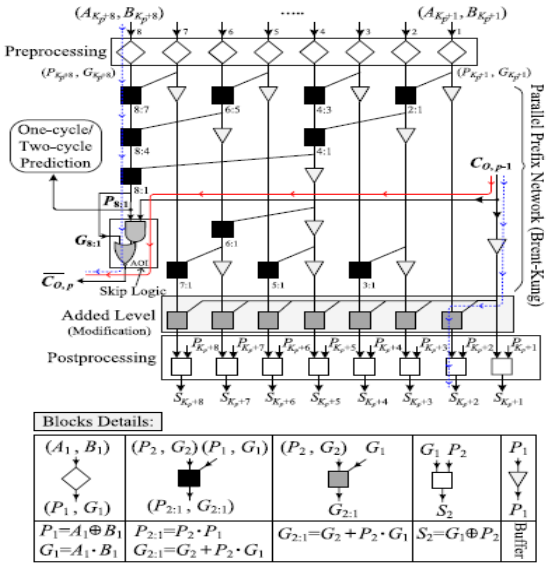


Fig.2 Internal structure of the *p*th stage of the existed hybrid variable latency CSKA.

As shown in the figure, in the preprocessing level, the propagate signals (*Pi*) and generate signals (*Gi*) for the inputs are calculated. In the next level, using Brent–Kung parallel prefix network, the longest carry (i.e., *G*8:1*)* of the prefix network along with *P*8:1, are calculated sooner than other intermediate signals in this network which is the product of the all propagate signals of the inputs. The signal *P*8:1is used in the skip logic to determine if the carry output of the previous stage (i.e., *CO,p*−1*)* should be skipped or not. In parallel with other stages all of these operations are performed and this signal is exploited as the predictor signal in the variable latency. In the case, where *P*8:1 is one, *CO,p*−1 should skip this stage predicting that some critical paths are activated. On the other hand, when *P*8:1 is zero, *CO, p* is equal to the *G*8:1.In addition, no critical path will be activated in this case.

The intermediate carries, which are functions of *CO,p*−1 and intermediate signals, are computed (Fig. 2) after the parallel prefix network. Finally, in the post processing level, the output sums of this stage are calculated. It should be noted that this implementation is based on the similar ideas of the concatenation and incrimination concepts used in the CI-CSKA. It should be noted that the end part of the SPL1 path from *CO,p*−1 to final summation results of the PPA block and the beginning part of the SPL2 paths from inputs of this block to *CO,p* belong to the PPA block (Fig. 2). The first

point of SPL1 is the first input bit of the first stage, and the last point of SPL2 is the last bit of the sum output of the incrementation block of the stage Q which is similar to the proposed CI-CSKA structure. Since the PPA structure is more efficient when its size is equal to an integer power of two, we can select a larger size for the nucleus stage accordingly.

The decrease in the number of stages as well smaller delays for SLP1 and SLP2 is leaded by the large size (number of bits), compared with that of the nucleus stage in the original CI-CSKA structure . Thus, the slack time increases further.

III PROPOSED SYSTEM

In this system we use nuclear stages. In nuclear stages we have preprocessing, parallel prefix network and post processing. One parallel prefix network is connected to other parallel prefix network through a skip logic. By using this proposed Hybrid Variable Latency the operation of the circuit is very fast.

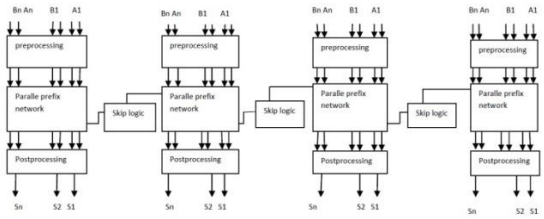
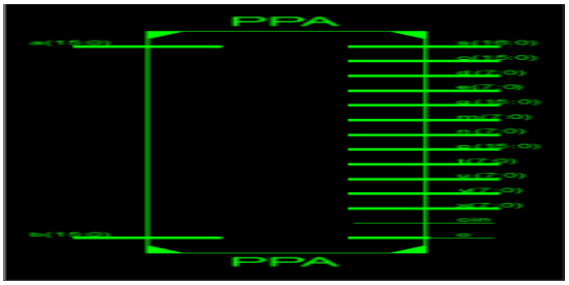


Fig.3 Structure Of The proposed Hybrid Variable Latency

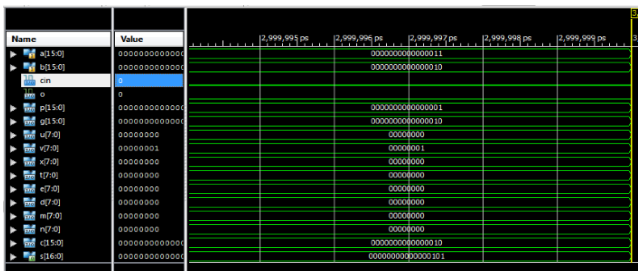
The skip logic is connected to interconnected blocks for every set of bits to make skipping operation at middle of the bits.

IV. RESULTS

RTL SCHEMATIC



OUTPUT



V CONCLUSION

In this paper, a static CMOS CSKA structure called CI-CSKA was proposed, which exhibits a higher speed and lower energy consumption compared with those of the conventional one. In this paper, a new approach to design a P.P adder concentrates on gate levels to improve the speed and decreases the memory. To speed up the binary addition it is like tree structure and cells in the carry generation stage are decreased. The great advantage in reducing delay is offered by the proposed adder addition operation. The lowest delay and PDP making itself as a better candidate for high-speed low-energy applications is showed by the suggested structure.

REFERENCES

[1] Pakkiraiah. Chakali, madhu Kumar. Patnala "Design of high speed Ladner - Fischer based carry select adder" IJSCE march 2013

[2] Haridimos T.Vergos, Member, IEEE and Giorgos Dimitrakopoulos, Member, IEEE," On modulo 2n +1 adder design" IEEE Trans on computers, vol.61, no.2, Feb 2012

[3] David h, k hoe, Chris Martinez and Sri Jyothsna vundavalli "Design and characterization of parallel prefix adders using FPGAs", Pages.168-172, march2011 IEEE.

[4] K. Vitoroulis and A.J. Al-Khalili, "performance of parallel prefix adders implemented with FPGA technology," IEEE Northeast Workshop on circuits and systems, pp.498-501, Aug 2007.

[5] Giorgos Dimitrakopoulos and Dimitris Nikolos, "High Speed Parallel Prefix ...Ling adders," IEEE Transactions on Computers, vol.54, no.2, February 2005

GHERA SUVARNA RATNA studied B.tech at malineni lakshmaiah women's engineering college during 2010 to 2014.At present she is pursuing M.tech at malineni women's engineering college. Her area of interest is VLSI design.

YENUGULA BHASKARA RAO studied M.tech at bapatla engineering college. At present he is working as associate professor at malineni lakshmaiah women's engineering college with 10 years experience.His area of interest is VLSI.