

# A Novel Dynamic Comparator with Reduced Kickback Noise

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**Abstract**—CMOS Dynamic latched comparators are preferred because they use Positive feedback mechanism with two back-to-back cross coupled inverters to convert a small input voltage difference to a supply voltage level in a short time. In this paper we adopted a kickback noise reduction technique which uses Exclusive OR gate in between regenerative nodes and inputs. To validate the results of our proposed design, it was compared with previous works like Single-tail Dynamic Comparator and Double-tail Dynamic Comparator using Mentor Graphics Design Tool with 130 nm technology. The proposed design can be used for the application of SAR ADC in Implantable Biomedical Devices.

**Index Terms**—Kickback noise, single tail dynamic comparator, and double tail dynamic comparator.

## I. INTRODUCTION

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Analog to Digital Converters (ADC), like Flash ADC, Sigma Delta ADC, Dual Slope Converters and Successive Approximation Register (SAR), provides a best choice in many special fields, such as Wireless Sensor Networks, Signal Acquisition Systems, Signal Processing Systems and Implantable Biomedical Devices.

In this paper, a dynamic comparator is designed for SAR ADC that can be used for the application of Implantable Biomedical Devices. Implantable Biomedical Devices, which are to be implanted in the human body, requiring extremely low power consumption to operate nearly 10 years or more.

ADCs are among the most critical and power hungry components of medical implant devices for measurement of various electro-physiological signals. Therefore, compared to other ADC architectures, SAR ADC has the advantage of simple structure, the least usage of analog circuit, and energy efficiency. In addition, SAR ADCs are compatible with increasingly scaled-down technology and can operate with ultra-low power supply.

In this paper, a comprehensive comparison about the power dissipation and Kickback noise of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [1], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional single tail dynamic comparator and double-tail comparator.

The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of each structure are discussed. The proposed comparator is presented in Section III. Simulation results are addressed in Section IV, followed by conclusions in Section V.

## II. CLOCKED REGENERATIVE COMPARATOR

Clocked regenerative comparators have found wide application in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from various aspects, such as Power dissipation, noise [2], offset [3], random decision errors [4], and kickback noise [5]. In this section, a comprehensive operation is presented; the power dissipation and kickback noise of two common structures, i.e., conventional single-tail comparator and conventional double-tail comparator are presented, based on which the proposed comparator will be presented.

### A. Conventional Single-tail Dynamic Comparator

The schematic diagram of the conventional Single-tail dynamic comparator widely used in ADCs, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig.1 [8]. The operation of the comparator is as follows. During the reset phase when CLK=0 and Mtail is off, reset transistors (M7-M8) pull both output nodes Outn and Outp to V<sub>DD</sub> to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK=1, transistors M7 and M8 are off, and Mtail is on. Output voltages Outp and Outn which had been pre-charged to V<sub>DD</sub>, start to discharge with different discharging rates depending on

the corresponding input voltage (INN, INP). Assuming the case where  $V_{INP} > V_{INN}$ , Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to  $V_{DD} - |V_{thp}|$  before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If  $V_{INP} < V_{INN}$ , the circuits work vice versa.

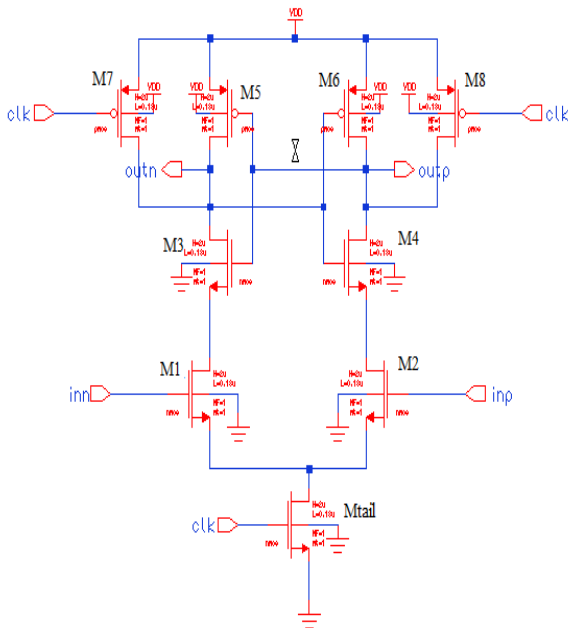


Fig. 1 Conventional Single-tail Dynamic Comparator

In principle, this structure has the advantage of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [8]. Since the parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate-source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower transconductances.

Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current of both the differential amplifier and the latch (the cross-coupled inverters). A large tail current would be desirable to enable fast regeneration in the latch[1]. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

#### A. Conventional Double-tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 2 [1]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional single-tail dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage ( $V_{cm}$ ), and a small current in the input stage (small Mtail1), for low offset[1].

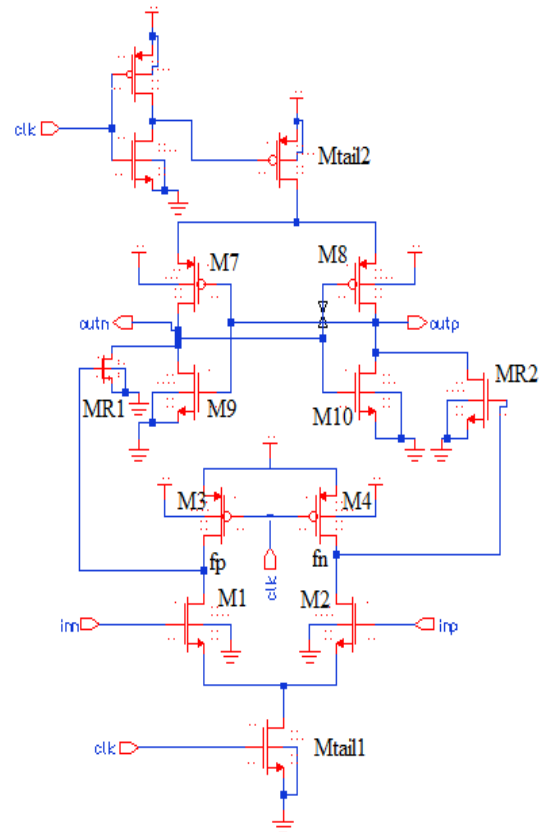


Fig. 2 Conventional Double-tail Dynamic Comparator

The operation of this comparator is as follows, during reset phase (CLK=0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK=1, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by  $I_{Mtail1}/C_{fn(p)}$  will build up. The intermediate stage formed by MR1 and MR2 passes  $\Delta V_{fn(p)}$  to the cross-coupled inverters and provides a good shielding between input and output, resulting in reduced value of kickback noise.

In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes must charge from ground to VDD, which means power consumption.

**B. Kickback noise**

Principally in latched comparators, the large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called “Kickback noise”.

The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

**III. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR METHOD**

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to avoid the uncertainty in the decision near the cross over points of INN and INP, where the noise caused the comparator to random decisions.

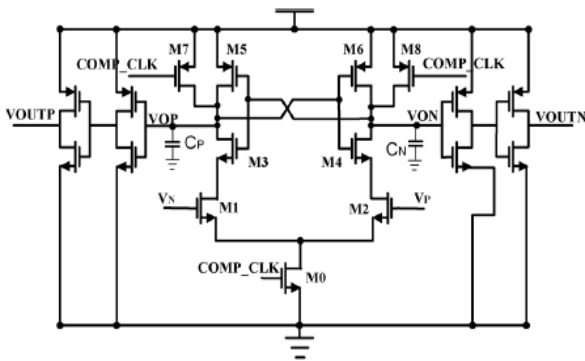


Fig. 3 Proposed Double-tail Dynamic Comparator with Kickback noise reduction technique

In this work, because all the capacitors are connected in parallel on the same side to perform the function of sample-and-hold, the total capacitance is large enough to suppress the  $kT/C$  thermal noise. In addition, the input-equivalent noise of the comparator also has the form of  $kT/C$ . The post-layout extraction shows that capacitance at the comparator outputs is 13.3 fF. Therefore, the input-equivalent noise of the comparator can be estimated to be 0.33 mV. Note that one LSB in this design is about 1.2 mV due to the top-plated sampling, and so input-equivalent noise of the comparator has the same order of magnitude as the quantization noise. Additionally, the input-referred offset voltage of a dynamic comparator is another key performance metric, which directly affects the system performance of a SAR ADC. Since devices mismatch due to process variation becomes worse, the input-referred offset voltage is getting much worse as technology scales

The analysis is made at the time point when “COMP\_CLK” reaches VDD and the circuit maintains a balanced steady-state. Here, balanced steady-state means

that currents in both branches are identical, and that at this point, M1-M6 are all in the weak-inversion region. The relationship between drain current and gate-to-source voltage of the transistor in the weak-inversion region

**IV. SIMULATION RESULTS**

To compare the proposed comparator with the conventional single-tail and double-tail dynamic comparators, all circuits have been simulated in a 130 Nanometer CMOS technology with VDD=1V using Mentor Graphics Tool.

TABLE I Performance Comparison

Comparator Structure	Power Dissipation	Kickback Noise
Conventional Single-tail dynamic comparator	604.8654 pW	1766.0834 $\mu$ V
Conventional Double-tail dynamic comparator	1.0049 nW	526.0242 $\mu$ V
Proposed Double-tail dynamic comparator with reduced Kickback noise technique	3.6585 nW	85.3582 $\mu$ V

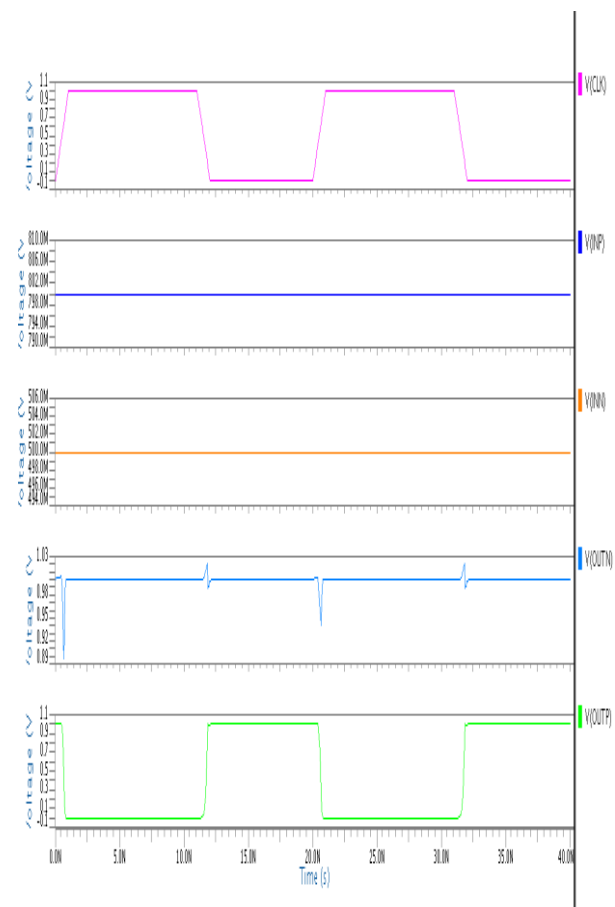


Fig. 4 Transient response of Conventional Single-tail Dynamic Comparator

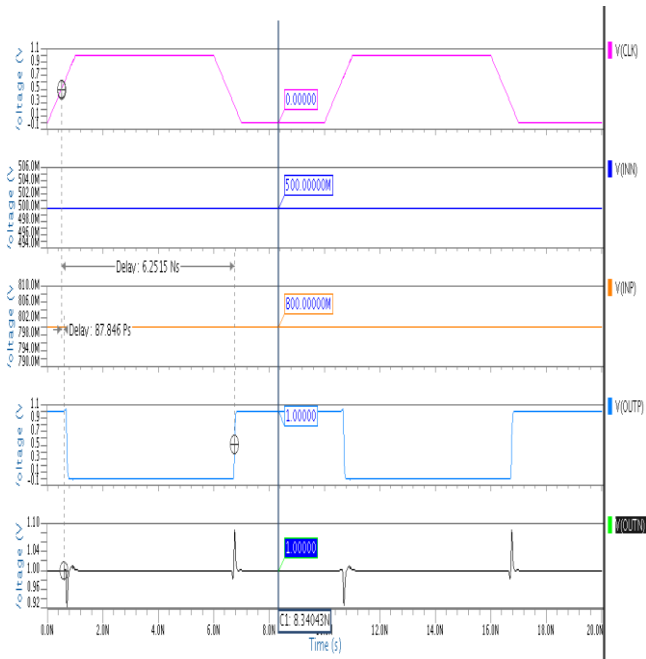


Fig. 5 Transient response of Conventional Double-tail dynamic comparator

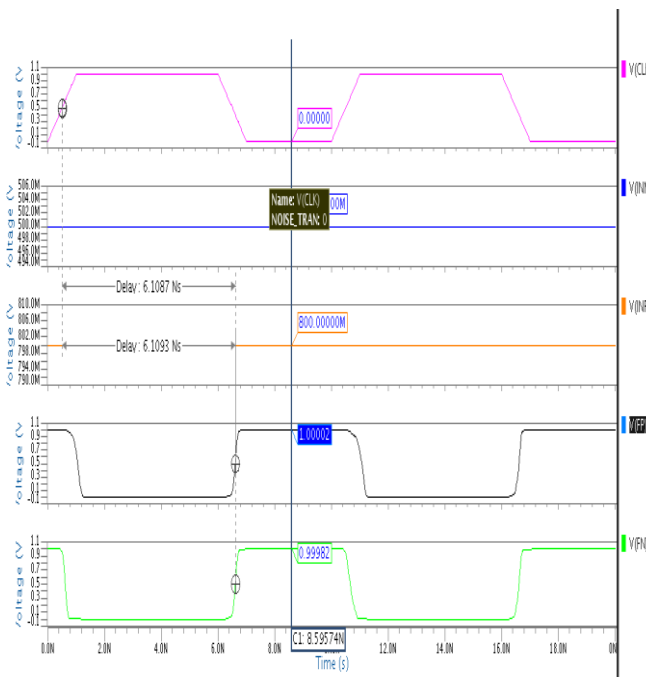


Fig. 6 Transient response of Proposed Double-tail dynamic comparator

### V CONCLUSION

In this paper, we presented a comprehensive Kickback noise comparison for clocked dynamic comparators with simulation results. Two common structures of conventional Single-tail dynamic comparator and Double-tail comparator were simulated. Also, based on simulation results, a new dynamic comparator with reduced Kickback noise was proposed to improve the performance of the comparator. In [6], it has been shown that the fastest and most power efficient comparators generate more Kickback noise. This is true about our

proposed dynamic comparator. Although it reduced the Kickback noise but power dissipation is increased in comparison to conventional double-tail comparator structure.

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