FPGA Implementation of Quadrature sampling Digital IF FM Receiver

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Abstract—In this paper FPGA implementation of resource efficient FM demodulation using quadrature sampling technique has been presented for digital FM radio receiver applications. The proposed demodulation design utilizes minimal number of hardware resources, caters to low-power receiver designs and provides high performance with digital IF filter for narrow bandwidth FM signal. FM signal at the receiver front-end is down converted to intermediate frequency signal (F_{IF}) and then digitized at a sampling rate less than the Nyquist frequency enabling Digital Down Conversion (DDC) for generating new intermediate frequency (f_{IF}), greater than the bandwidth of the modulating signal. A fixed point arithmetic based digital demodulation is then performed using proposed quadrature demodulation architecture. The hardware design implementation of the design is carried out in ProASIC3E-A3PE1500 Flash FPGA. Implementation results show maximum operating frequency of 68.3 MHz and gate utilization of 1453 core logic cells (4 percent device utilization) of the targeted device for the proposed demodulation algorithm.

Index Terms— Band pass sampling, Digital demodulation, Digital FM Receivers, Digital down conversion (DDC), Field Programmable Gate Array (FPGA), Fixed point arithmetic, Quadrature sampling, Arc tan demodulation.

I. INTRODUCTION

Traditional FM demodulators designed using analog circuits like limiter discriminator integrated circuits or PLL circuits are being replaced by digital signal processing techniques with state of art device technologies like FPGAs and DSP processors. With recent advancements in high speed and high resolution analog to digital converters and digital signal processing algorithms, custom made receivers with desired selectivity and high performances can be implemented using FPGA based technology. Conventional techniques for FM demodulation include coherent demodulation using PLL plus VCO and non-coherent methods like slope-detection and quadrature demodulation. Fig.1 below shows a conventional architecture for FM demodulation using I/Q extraction.

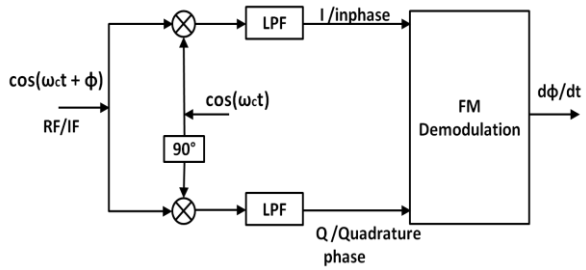

Fig.1 Conventional quadrature demodulation architecture

This paper proposes hardware architecture for the FPGA implementation of FM demodulation for digital IF receivers using quadrature sampling technique. The usage of band pass sampling technique and sampling frequency selection for narrow bandwidth FM receiver are discussed. The paper also describes the aliasing effect due to sub sampling procedure and requirement to have digital IF FIR filter after digitization of IF signal.

The present paper is organized as follows. Section II describes the FM modulated signal, IF filter requirements, quadrature sampling and demodulation algorithm of FM signals in digital FM receivers. Section III dwells on the proposed hardware implementation of demodulation architecture in FPGA. Section IV gives the synthesis and simulation results. Resource utilization, power consumption and maximum operating frequency for the proposed design are provided. The final conclusion and discussions are provided in section V.

II. THEORY

Non-linear modulations like angle modulation schemes used in communication systems are known for their high degree of noise immunity with trade-off for bandwidth. FM modulation is a type of angle modulation in which frequency of carrier signal is a function of modulating signal. The instantaneous frequency of the carrier signal varies linearly with modulated message signal.

An FM modulated signal [1] in general can be written as

$$S_{FM}(t) = A_c \cos[2\pi f_c t + \theta(t)] \quad (1)$$

$$= A_c \cos[2\pi f_c t + 2\pi K_f \int_0^t m(\tau) d\tau] \quad (2)$$

where A_c is the amplitude of the carrier, f_c is the carrier frequency, m(t) is the message signal and K_f is the frequency deviation constant. A typical FM receiver consist of RF Front end and demodulator. Fig.2 shows the digital RF receiver architecture[6] with RF front-end comprising of amplifiers, down converters and filter and digital demodulator.

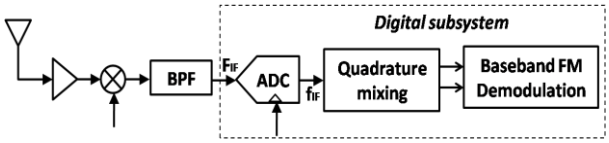

Fig.2. Digital Radio Receiver

For the given FM signal as in equation (1) and in the conventional *quadrature demodulation* architecture shown in fig.1,

The output signals (I & Q) after mixing process are:

$$\begin{aligned} I_{fm}(t) &= S_{FM}(t)*\cos(2\pi f_c t) \\ &= A_c \cos\left[2\pi f_c t+\theta(t)\right]*\cos(2\pi f_c t) \\ &= \frac{A_c}{2}\cos\left[\theta(t)\right]+\frac{A_c}{2}\cos\left[4\pi f_c t+\theta(t)\right] \end{aligned} \tag{3}$$

$$\begin{aligned} Q_{fm}(t) &= S_{FM}(t)*\sin(2\pi f_c t) \\ &= A_c \cos\left[2\pi f_c t+\theta(t)\right]*\sin(2\pi f_c t) \\ &= \frac{-A_c}{2}\sin\left[\theta(t)\right]+\frac{A_c}{2}\sin\left[4\pi f_c t+\theta(t)\right] \end{aligned} \tag{4}$$

Low pass filter are necessary after the mixing operation to eliminate the second harmonic of the carrier and generate the inphase and quadrature phase data. The proposed approach of I and Q generation eliminates the need to have low pass filters which is required in the conventional demodulation designs.

The digital subsystem block diagram presented in this paper is shown in Fig.3 below.

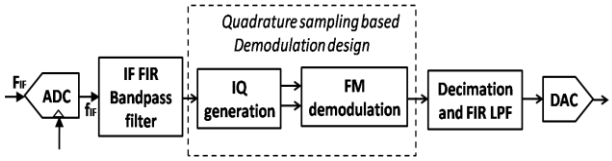

Fig.3.Digital subsystem block diagram

In the proposed method, the intermediate frequency (F_{IF}) of constant amplitude obtained from the front-end is sampled at rate less than the Nyquist rate ($2F_{IF}$). As per band pass sampling theorem[2], the conditions for acceptable uniform sampling rates for band pass signals are

$$\frac{2f_u}{n} \le f_s \le \frac{2f_L}{n-1} \tag{5}$$

where f_s is the sampling frequency, n is the integer given by $1 \le n \le \left\lfloor \frac{f_u}{B} \right\rfloor$, B is the bandwidth of the message signal, f_u and f_L are upper and lower frequency contents of the band pass signal as shown in Fig.4.

A. Quadrature Sampling

For Quadrature demodulation[2], the inphase and quadrature phase components can be sampled explicitly from band pass signal if the intermediate frequency (F_{IF}) is sampled with sampling duration of *k* sec as follows:

$$k = \frac{1}{4f_c} \pm \frac{m}{2f_c} \tag{6}$$

or equivalently, $f_s = \frac{4f_c}{2m \pm 1}$ (7)

where m=0,1,2,3 .... and $f_c = F_{IF}$ is the center frequency of the IF signal to ADC.

For a simple case of $m=1$ and $f_s = \frac{4F_{IF}}{3}$, the obtained data stream from the output of analog to digital converter gives original IF sampled at 90º intervals. If we assume the first sample at 0º as I, the subsequent sample at 90º is Q, the next sample at 180º is -I and following sample at 270º is -Q and cycle repeats itself. The separation mechanism for I and Q in FPGA is done using 1:2 multiplexer, a divide by two clock and alternate multiplication of +1 and -1 to avoid the phase reversal of the samples as shown in fig.6 in section III.

The I/Q generation from consecutive ADC sample data is shown below:

$$S_{FM}(n) = A_c \cos\left[2\pi f_c n T_s + \theta(nT_s)\right] \tag{8}$$

where $T_s = \frac{1}{F_s} = \frac{3}{4f_c}$ and $f_c = F_{IF}$

$$S_{FM}(n) = A_c \cos\left[\frac{3\pi n}{2} + \theta(nT_s)\right] \tag{9}$$

For n=0, 1,2,3 respectively ,

$$S_{FM}(0) = A_c \cos\left[\theta(0)\right] = I \tag{10}$$

$$S_{FM}(1) = A_c \cos\left[\frac{3\pi}{2} + \theta(T_s)\right] = A_c \sin\left[\theta(T_s)\right] = Q \tag{11}$$

$$S_{FM}(2) = A_c \cos\left[3\pi + \theta(2T_s)\right] = -A_c \cos\left[\theta(2T_s)\right] = -I \tag{12}$$

$$S_{FM}(3) = A_c \cos\left[\frac{9\pi}{2} + \theta(3T_s)\right] = -A_c \sin\left[\theta(3T_s)\right] = -Q \tag{13}$$

B. Digital IF FIR filter

The sampled spectrum is periodic in nature. The sub sampling procedure introduces the noise aliasing, spurious

signal aliasing into the nyquist zone of the desired FM signal (usually first nyquist zone) in addition to spurious signal generation by ADC in the first nyquist zone. This aliasing effect apart from quantization noise degrades the carrier to noise ratio in the digitized signal thus putting a limitation on signal to noise ratio of demodulated output.

An IF Bandpass filter with linear phase characteristics in desired passband is essential for frequency component selection in the first nyquist zone and also to attenuate the spurious and image frequency components after the subsampling process.

Fig.4 below shows amplitude spectrum for the aliasing phenomena and IF filtering. The figure shows rise in the noise floor of the spectrum due to foldback.

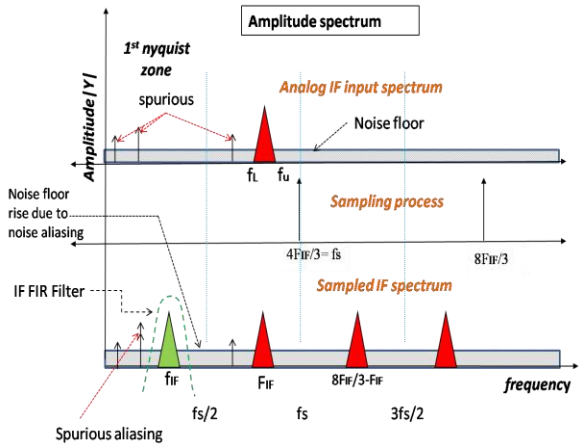

Fig.4.aliasing and filtering for the quadrature sampling process

An FIR band pass filter[3] with bandwidth approximately equal to message signal bandwidth and having pass band centre frequency equal to digitized intermediate frequency (f_{IF}) overcomes the signal-to-noise ratio degradation.

A transposed form of FIR filter architecture with fixed point arithmetic is implemented in the design.

C. Demodulation algorithm

The instantaneous phase of received FM signal is derived using Arc tan demodulation algorithm [4] from sampled I and Q samples. Fig.5 shows the phase extraction of FM signal using Arc tan method.

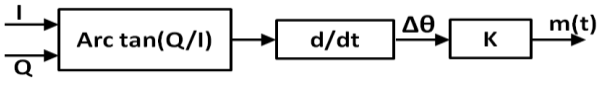

Fig.5 Arc tan method of instantaneous phase determination

$$r(t) = q(t)/i(t) \tag{14}$$

$$\Delta\theta = \frac{d(Tan^{-1}[r(t)])}{dt} = \frac{1}{1+r^2}\frac{d[r(t)]}{dt} \tag{15}$$

$$\frac{d[r(t)]}{dt} = \frac{i(t)\dfrac{d[q(t)]}{dt} - q(t)\dfrac{d[i(t)]}{dt}}{i^2(t)} \tag{16}$$

In discrete domain, the equation (15) using first order approximation of taylor series for differentiator operation can be reproduced as,

$$\Delta\theta(n) = \frac{i(n)[q(n)-q(n-1)]-q(n)[i(n)-i(n-1)]}{i^2(n)+q^2(n)}$$

$$= K[q(n)i(n-1)-i(n)q(n-1)] \tag{17}$$

where $K = \dfrac{1}{i^2(n)+q^2(n)}$

after extracting the baseband signal, decimation process is carried out followed by digital low pass filter as illustrated in fig.3.

III. HARWARE ARCHITECTURE

Fig.6 describes the IQ extraction mechanism using quadrature sampling technique implemented in the design.

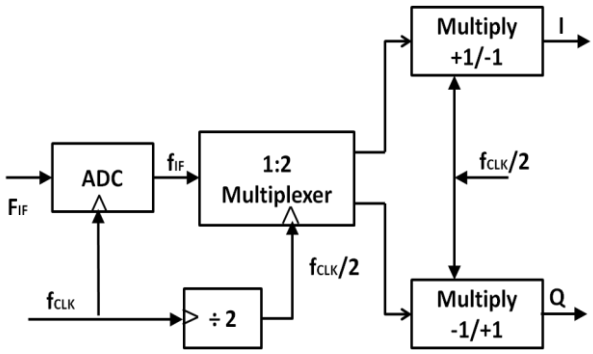

Fig.6. IQ sample generation

where $f_{CLK} = \dfrac{4F_{IF}}{3}$, from equation (7) and $f_s = f_{CLK}$

The f_{IF} is the fold back frequency ($f_{CLK}/4$) of F_{IF} arriving in the first nyquist zone. The sampling process is carried out to give fixed point 2's complement data at the ADC output which is fed to FPGA. The sampled data stream are separated alternately using a 1:2 multiplexer utilizing a divide by 2 clock scheme. The multiplication operation by -1 is performed by generating two's complement of the sample.

The demodulation process for the generated IQ samples is carried out as per equation (17).The block diagram in Fig.7 reflects the equation.

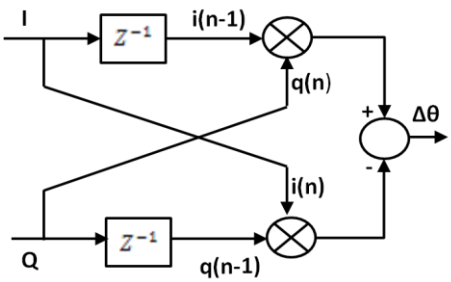

Fig.7 Block diagram of FM demodulation

The delay operation is performed using shift registers. 12 bit fixed point multiplication is implemented . The input I and Q are 12 bit 2'complement format and the output of multiplication operation results in 24 bits. The final output of the demodulation having 24 bits is truncated to 12 MSB bits.

IV. Implementation Results

A. Synthesis Results

The proposed demodulation architecture has been implemented using VHDL hardware description language using ***Microsemi Libero IDE 9.0*** software. The synthesis of the design has been done with ***ProASIC3E-A3PE1500*** Flash FPGA as the target device. ***Synplify*** software tool is used for design synthesis. Simulation of the code has been carried using ***Mentorgraphics ModelSim 6.5*** with the test vector of FM signal having carrier frequency of 10.7 MHz and 12 bit two's complement format. The ADC output is a 12 bit fixed point two's complement format and having output data rate of $4F_{IF}/3$, which is 14.2667 MSPS for 10.7MHz IF input.

Table.1 below provides the typical power consumption analysis of implemented hardware architecture as described in section III and targeted for ProASIC3E-A3PE1500 device. The power analysis is carried out using smart grid tool of ACTEL designer software suite after placing and routing and layout generation. Table.2 provides the resource utilization and timing summary.

Table.1 Power analysis

Power consumption summary	
Static power	17.82 mW
Dynamic power	40.466mW
Total power	58.296mW

Table.2 Synthesis summary

Summary	
Max operating clock frequency	68.3MHz
Core cell usage	1453 of 38400 (4%)

B. Simulation results

The functional simulation of the proposed demodulation technique is carried out in MATLAB and Mentor Graphics MODELSIM HDL simulation software. Fig.8 shows the simulated waveform of the input 10.7MHz signal sampled at 14.2667MHz and Fig.9 shows the demodulated 15 kHz output signal. The frequency deviation of the FM signal test vector is 30kHz.

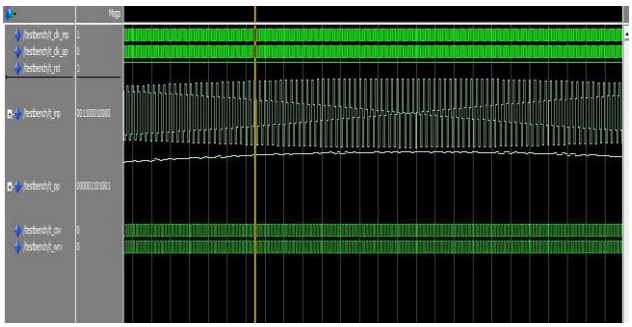

Fig.8. FM modulated signal waveform in MODELSIM

Fig.10 shows the demodulated signal of 15kHz tone and its spectrum with digital FIR LPF after demodulation captured in oscilloscope.

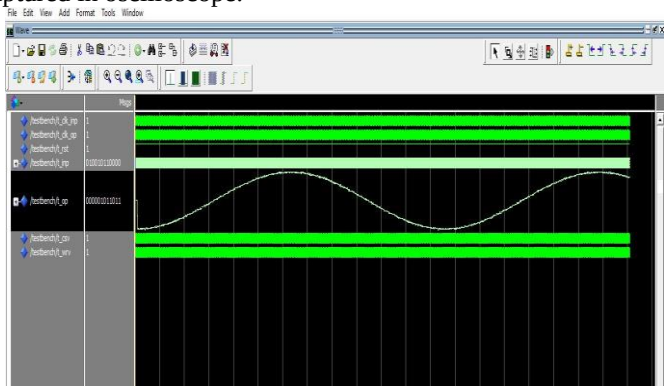

Fig.9. Demodulated signal waveform in MODELSIM

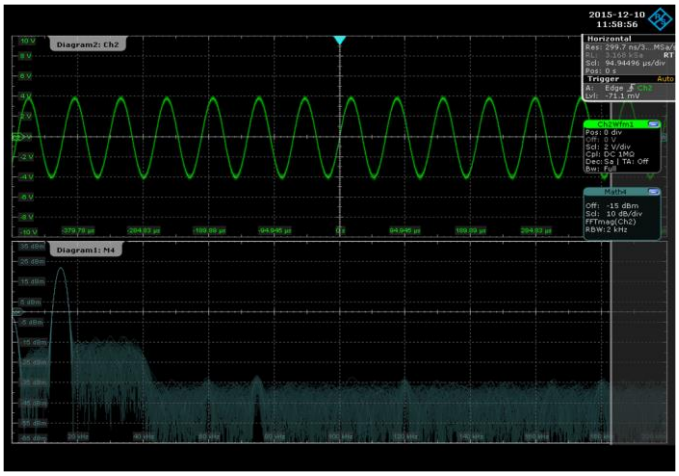

Fig.10. time domain and frequency domain demodulated output after DAC

V. CONCLUSION

A new approach for demodulation of FM signal which utilizes minimum hardware resources is proposed in this paper. The multipliers and look up tables utilized for the mixing operation in conventional technique are avoided in this implementation. The FPGA design targeted towards ProASIC3E Flash FPGA provides the demodulation operation with low-power consumption and utilizes 4 percent of the device resources. The I and Q samples generated in the proposed design provides optimal performance results for bandwidth of the message signal considerably less than the centre frequency. The sampling frequency (f_s) provided in equation (7) gives exact 90° phase between consecutive samples. Minimal drift in ADC sampling is required to have negligible quadrature phase shift errors and to deliver distortionless demodulated output.

VI. ACKNOWLEDGEMENT

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