I A survey on Electromagnetic Aspects in Integrated Circuits

Dr. K. BIKSHALU[1*]
Department of Electronics and Communication Engineering
University College of Engineering
Kakatiya University
Kothagudem, Telangana, India
E-mail: kalagaddaashu@kakatiya.ac.in

PRATHAP SOMA [2]
Assistant Professor of ECE
CVR College of Engineering, Hyderabad, India
E-mail: prathap.soma@gmail.com

***Abstract*—The achievement of high speed IC technology is possible only with a reduction in transistor size, increasing the number of interconnects (circuit complexity), scale down the power supply and high clock speed, these leads to electromagnetic emission thereby EM interference[1] problem raised. In earlier technologies the electromagnetic interference is controlled by maintaining the appropriate integrating circuit packages at chip level. The development of high performance ICs with low emission and high susceptibility can be obtained using various approaches. The objective of this survey- paper presents all possible electromagnetic aspects In IC like die size, heat sink, internal noise on DIE, and a mathematical model of representing simultaneous Switching Noise (SSN), Cross talk.**

***Index Terms*— SBGA, PBGA, EM interference.**

I.INTRODUCTION

Generally, based on the propagation approaches EMI noise generation is of 3 types

- Conducted EMI noise: due to high transient currents generated from digital core through the silicon track, bending wires and package lead frames.
- Capacitive/inductive EMI noise: Due to parasitic capacitance/inductance associated with transistor.
- Radiated electromagnetic wave noise: from Internal interconnects or from package frames

The main aim of this paper is to develop a high performance IC with low emission and high susceptibility. Various approaches involved in increasing the susceptibility of ICs. One of the approaches is the 3D IC technology where the die size of the circuit is negligibly small compared with traditional IC technologies. Another possible approach is adding the global communication network to the ICs.

Adding of on chip global communication [2] network is of 2 types.

1. Micro strip transmission line based interconnects operating in the RF range:
   It has been found that the majority of the wave propagation happens in the substrate and through surface waves. Since there are local metal interconnects present in the same metal layer as that of the antenna.
   Hence, it is critical to analyze the signal coupling between the antenna and the metal interconnects. Since the metal interconnects are essentially micro-strip elements, the signal coupling depends on the dimensions of interconnect.
   The signal coupling between the on-chip antennas and the metal interconnects can be characterized for varying width, length and placement of the metal interconnect. It is also possible to have a good electromagnetic compatibility for the on-chip antennas.
2. Wireless communication based intra-chip interconnects operating in RF communication: with this technology the effect of radiation on MOSFET devices is very small and can be neglected.

II. DIFFERENT ASPECTS IN IC'S

With emerging IC technology, EMI problem is also increased. The main causes of Electromagnetic emission involves die size, heat sink, internal noise on DIE, and a mathematical model of representing simultaneous Switching Noise (SSN), Cross talk. This chapter gives the mathematical relationship between EM emissions with various parameters.

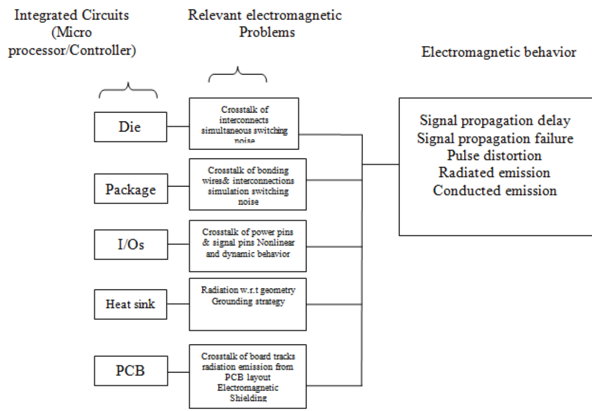

Figure 1: Different EMI/EMC effects on IC

A. CROSS TALK

It is a very common problem in IC design. Mainly occurred due to undesired signal transmitted by the one of transmitting circuit (source) with its faulty behavior of another circuit (victim) considered as input. Thereby interference takes place. Generally, cross talk is expressed in dB.

Crosstalk=20log (Vs/Vc) in dB

Where Vs source voltage and Vs victim voltage

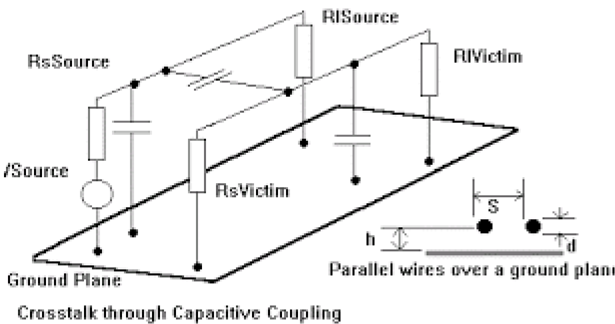

Figure 2: Crosstalk in IC's

In IC technology, as the circuit dimensions scaled the gap between the source and victim is also scaled which contributes to an increase crosstalk noise. This consequently affects IC performance. Above fig.6 shows the crosstalk effect through parasitic capacitance coupling which influence the behaviour of IC. Hence the fraction of parasitic capacitance plays major role in the performance of the IC's. The crosstalk noise can be reduced by maintaining the proper timing constraints, Buffer planning and adjusting the driving gate size during the floor planning.

B. SIMULTANEOUS SWITCHING NOISE (SSN)

This is referred as noise or ground bonus. It is another parasitic effect caused by the simultaneous switching of million internal transistors. With this a strong current generated at the digital core level thereby operating frequency is increased. This noise is proportional to the inductor (L) and rate of change of current between device ground and system ground.

i.e.,

$$V=L\,di/dt$$

Therefore, faster current switches greater drop voltage. Understanding of SSN is explained with the help of a simple CMOS inverter [3]. When there is a transition from logic '0' to logic '1' or '1' to '0' there exists transient current in the pull down and pull up network. These transient currents are function of the number of logic cells in an IC, means that transient current increases with number of logic cells.

The SSN has affected more on circuit performance. These affects have majorly occurred in:

1. Produces glitching power dissipation in lower networks.
2. Decrease the gate driven strength
3. Reducing the overall system gain.

Simple mathematical expression of electromagnetic interference related to switching noise or transient noise is explained below.

Following the results of SSN are measured by reducing delay with varying the values of capacitances and inductances.

In fig.4 when input voltage is at logic '1' the NMOS transistor ON and has operated in the saturation region. Therefore the current through the NMOS transistor is given by

$I_N = Bn\,(Vin-V_{TN}-Vs)^{n}$ ----------------------1

SSN voltage can be represented as

$Vs=R\,I_L+L\,(dI_L/dt)$ ----------------------------2

Can also define current through parasitic inductance as

$I_L=I_N - C\,(dV_s/dt)$ ------------------------------ 3

Assuming that the magnitude of Vs is very small compared to $V_{IN}-V_{TN}$, Therefore I_N can be rewritten as

$I_N=B_n\,(V_{IN}-V_{TN})^{n}-dI_N/dV_{Gs} * V_s$ --------------------4

Derivative I_N with respect to V_{Gs}

$f1=dI_N/dV_{Gs}= nB_n\,(V_{IN}-V_{TN} - Vs)^{n-1}$-------------------5

Here f1 is function of $V_{Gs.}$ In order to simplify the above derivative function f1 using V_{IN} equal to 0.5 Vdd

Therefore eq.5 can be modified as

$= L_{Vss}\,Cv_{ss}\,d^2Vs/dt^2 + (R_{Vss}C_{Vss}+L_{Vss}f1)\,dVs/dt$

$+ (RV_{ss}f1+1)\,Vs$

$\simeq R_{Vss}B_n(V_{IN}-V_{TN})^{n} +L_{Vss}\,d/dt[B_n(V_{IN}-V_{TN})^{N}]$

The first term $L_{Vss}\,Cv_{ss}\,d^2Vs/dt^2$ is neglected because of all other components are dominated.

$(R_{Vss}C_{Vss}+L_{Vss}f1)\,dV_s/dt+ (RV_{ss}f1+1)\,Vs$

$\simeq R_{Vss}B_nV^{n}_{dd}\,(t/\tau_r-Vn)^{n} +L_{Vss}BnV^{n}_{dd}/\tau_r\,[(t/\tau_r -V_n)^{n-1}]$

Here $Vn=V_{TN}/V_{dd}$ because of non integer values varies of n and n-1 analytical solution [4] exists therefore approximated expression for the differential equation of $(t/\tau_r-Vn)^{n}$ and $(t/\tau_r -V_n)^{n-1}$ with the average error of 3%

$Vs=C_0\,(1-e-^{(t-\tau n)/\gamma\tau r}) +c_1\xi+c2\xi^3+c3\xi^3+c4\xi^4+c5\xi^5$

For $\tau_n \leq t\leq \tau_r$

Figure 3: Measure instrument of shielding effectiveness of IC package.

Where, $\gamma= (R_{Vss}C_{Vss}+L_{Vss}f1)/ (RV_{ss}f1+1)\ \tau_r$

$\tau_n= V_{TN}*\ \tau_r/V_{dd}$

$c_0=A_0\gamma-A_1\gamma^2+2A_2\gamma^3-6A_3\gamma^4+24A_4\gamma^5-120A_5\gamma^6$

$c_1= A_1\gamma-2A_2\gamma^2+6A_3\gamma^3-24A_4\gamma^4+120A_4\gamma^5$

$c_2= A_2\gamma-3A_3\gamma^2+12A_4\gamma^3-60A_5\gamma^4$

$c_3= A_3\gamma-4A_4\gamma^2+20A_5\gamma^3$

$c_4== A_4\gamma-5A_5\gamma^2$

$c_5= A_5\gamma$

A_i for i=0, 1, 2,3,4,5 are

$A_i= [(R_{Vss}B_nV^n_{dd}\ \tau_r) / (R_{Vss}C_{Vss}+L_{Vss}f1)]\ a_i$
$+ [(LV_{ss}B_nV^n_{dd}) / (R_{Vss}C_{Vss}+L_{Vss}f1)]\ b_i$

The above equation indicates SSN voltage of CMOS inverter. Where, a_i,b_i are defined in[5].SSN voltages reaches maximum when input changes transitions at t= τ_r

C. PACKAGE TECHNOLOGY

Package technology is also one of the predominant effects on EMC. It is an essential part of an IC design, useful for protecting the device from external environment and provides isolation. It also protects the IC from electrical and electromagnetic effects. The Future is much concerned with different requirements in IC evolution.

There are two most used package techniques available at 10GHz frequency. They are

1. SBGA(Super Ball Grid Array)

2. PBGA (Plastic Ball Grid Array).

In early technologies by maintaining the appropriate integrating circuit packages they control the electromagnetic interference at chip level. Up to 10GHz PBGA and SBGA packages [6] are helpful. In these two cases SBGA packages are better compared with PBGA packages.

III. SHIELD EFFECTIVENESS VERIFICATION

The shield effectiveness verification of an IC package is based on GTEM technique. With this electromagnetic compatibility characteristics are verified.

Generally, two packages are involved in designing the IC's at 10GHz frequency. They are SBGA, PBGA.

The testing of packages is done with the help of GTEM [7] i.e., Gigahertz Transverse Electro Magnetic cell. Below Fig.1 shows GTEM cell Equipment. The internal setup involved in GTEM cell is depicted in fig.2.Which consist of an IC antenna based on feed connections which acts a dipole antenna results a current flow along the thin conductor tracks printed on a planar dielectric substrate. This is the primary test setup of High speed IC electromagnetic interference.

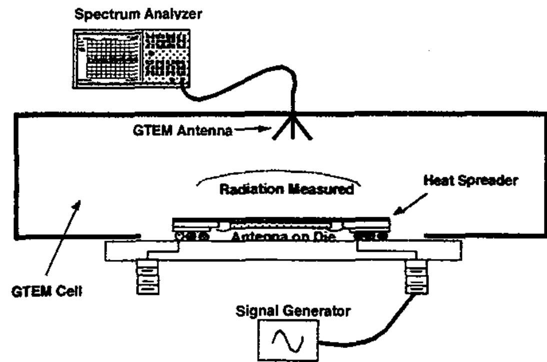

Figure 4: GTEM cell for emission and immunity testing

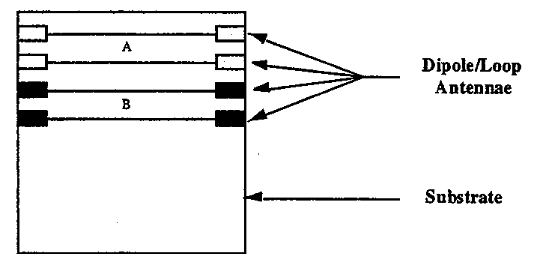

Figure 5: An IC antenna in GTEM

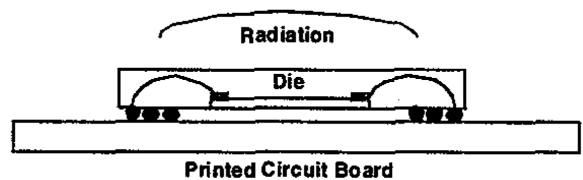

Figure 6: Structure of PBGA Package

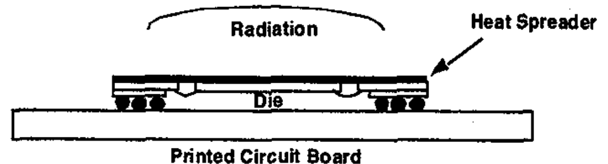

Figure 7: Structure of SBGA package.

The following procedure involved for finding the shielding effectiveness of an IC package.

1. The IC antenna is placed in reference package and excited with a sweep generator with suitable frequency range.
2. The radiated power is now collected at the opposite end of the GTEM cell and is measured form spectrum analyzer. Then same setup maintained for testing the Package under Test with the same conditions.

3. The difference between two recorded values gives information about the effectiveness of the IC package with respect to reference package.

This procedure is helpful for both SBGA, PBGA packages. As with the comparisons SBGA packages are affected less interference than PBGA packages.

D. HEAT SINK

In order to maintain constant temperature in an IC heat sink is used. Generally heat sink is mounted on the IC. As the IC size, scaled the heat sink size also scaled the small size heat sink (Based on its electrical size) may act as an antenna, which radiates electromagnetic coupled noise using a simplified heat sink model as a dipole antenna as the source of electromagnetic noise. Therefore the size of the antenna also plays major role in the EMC radiation. At high frequencies IC emit an excess amount of heat; therefore heat sink radiation is also taken into consideration. The study of circular antenna is so simple compared to mono pole antenna.

The entire effect of heat sink on IC is not removed. By Grounding the heat sink some portion of this effect is eliminated.

Based on the number of ground points grounding techniques are divided into different types.

They are 8 grounding posts technique and 4 grounding posts technique [8].

8 grounding posts technique means that the heat sink is grounded at 8 different locations and is used to suppress EM emission up to 6GHz where as 4 post ground technique is up to 1.5GHz.some research have been still searching the solution for removing the major EM problem associated with heat sink.

E. I/O AND PCB

The behaviour of individual input and output devices emission are also taken into consideration because these devices are interconnected to the IC. Therefore, researchers are not only focused on IC, also focused on I/O ports and their interconnects as well as on the PCB. Based on behavioural modelling and simulation methods are useful for estimate the noise in the mathematical model.

Whereas Radial base function (RBF) [9] or piecewise RBF model is employed for presentations. Out of this parametric model works accurately to estimate the EM noise radiated from the I/O and PCB.

III. FUTURE SCOPE

According to Moore’s law the transistor count is doubled for every 18 months this means that the development of ICs technology is very vast. The recent trends include microprocessors are designed with 50GHz and micro controllers are designed with 3GHz at 32 nanometre technology with increased speed of operation, consequently the EMC problem is also increased. Using of new frequency bands for an IC is the only one possible solution for preventing EMC radiation and increase the susceptibility of IC. Now researchers are should focus on new frequency bands its level of interference and susceptibility.

Considering all these effects, researchers and academicians should develop optimized and customized IC.

IV. CONCLUSION

Here it concluded that this paper gives enough information on an effect of electromagnetic interference on Integrated circuits. Such as packaging, die size, Heat sink, I/O and PCB with a mathematical relationship on SSN and crosstalk also included. This paper is helpful for researchers as well as academicians to know the hierarchy of EMC and EMI problems associated with IC technology.

REFERENCES

[1] IEC 61967: integrated circiuits, measurement of electromagnetic emission upto 1GHz, www.iec.ch

[2] D.Sylvester and K.Keutzer, “A global wiring paradigm for deep submicron design”,IEEE Transactions on Computer-Aided Design of Integrated Circuit and Systems, vol 19.pp.242-252,feb2000.

[3] Kevin T.Tang and Eby G.Friedman Fellow IEEE “simultaneous Switching Noise in On-Chip CMOS Power Distributed Networks” IEEE TRANSACTIONS ON VERY LARAGE SCALE INTEGRATION (VLSI) SYSTEMS VOL.10 NO.4 AUGUST2002

[4] A.Vaidyanath,B.Thoroddsen,and J.L. Prince,”Effect of CMOS driver loading conditions on simulataneous switching noise,” IEEE Transactions components, packaging, manuf.techol.-part B,vol.17, pp.480-485,Nov.1994.

[5] Y.Yang and J.R.Brews,”Design for velocity saturated,Short channel CMOS drivers with simulation switching noise and switching time considerations,” IEEE J.Solid-State circuits,vol.31,pp.1357-1361,sept.1996.

[6] J.J rollin, G.Arcari and L.Roy “EMC performance of IC packages”IEEE 1999.

[7] J.J rollin, L.Roy and G.Arcari “A novel technique for measuring IC package shielding effectiveness,” 16th IEEE instrumentation and measurement technology conference, venice,1999.

[8] Paul, C.R, Inroduction to Electromagnetic compatibility,Wiley interscience,Newyork,2010.

[9] Zhu Xizhi “Study of surface Electromyography Signal Based on wavelet transform and Radial Basis Function Neural Networks” IEEE conference on Future biomedical information engineering 2008.