VHDL DESIGN AND IMPLEMENTATION OF C.P.U BY REVERSIBLE LOGIC GATES

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Abstract*—Digital system implemented by using conventional gates like AND and OR gates dissipates a major amount of energy in the form of bits which gets erased during logical operations. This problem of energy loss can be solved by using reversible logic circuits in place of conventional circuits. Reversibility has become the most promising technology in digital circuits designing. In today's world C.P.U is one of the very important parts of any system having A.L.U applications for computers, cell phones, calculators etc. In this paper the design of 8-bit reversible C.P.U using reversible logic gates is proposed. The proposed C.P.U is analyzed on FPGA SPARTAN6 device. The proposed design is compared in terms of propagation delay, memory used and garbage outputs. In this paper the 8-bit reversible A.L.U and reversible logical unit is designed using Feyman, Peres, DKG and N.S gates. A memory block is designed with a row and coloumn addresses and organized to form a reversible C.P.U .

Keywords*—Reversible logic gatesr; N.S gate; Reversible processor; less power, martrix memory block.

I.INTRODUCTION

In the past decennary, great success have been made in the growth of computing machines. However, because of the exponential growth of transistor density and in particular because of the vastly increasing power dissipation, researchers expect that the conventional technologies like CMOS will reach their confines in the near future. To further fulfill the needs for more computational power, alternatives are technology having its use in quantum computing, nanotechnology, low power CMOS and optical computing. The main idea of designing reversible logic is to lower the quantum cost and garbage outputs by M.Thmosen[7]. Power dissipation is one of the most important problems in conventional technology. In 1961 Landauer[3] projected a computing device in order to bear the degrees of liberty will act as a heat sink for the energy required for calculation, resulting in computing errors. According to Landauer's principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k represents the Boltzmann's constant and value of k is 1.38x10 -23 J/K, T is the absolute temperature in Kelvin[2]. The primal combinational logic circuits dissipate heat energy for each bit of information that is lost during the operation. This is so because according to second law of thermodynamics, once the bit containing information get lost then it cannot be recovered by any approach or techniques. C. H. Bennett[2] proved that the dissipated power is straightly related to the number of bits which were lost during process, and also that the computers can be reversible logically, reduced complexity and at convenient speed generate précised calculations and to avoid kTln2 joules of energy dissipation in a circuit it should be made from reversible circuits. For this the circuit must be logically reversible. A new approach of design comes in the field of digital circuits designing for limiting the power dissipation. The device designed according to this new approach is known as a *Reversible Logic Device.* A gate designed using reversible logic is called Reversible Logic Gate. Inputs are determined by the programmers for execution in an instruction set architecture. Based on these input arithmetic logic units should be able to generate variety of logic outputs. Hence in this type of environment reversible logic circuits must have both fixed select input lines that receive op code signals determined by programmer and output lines where the logical output result is produce.

ARITHMETIC AND LOGICAL UNIT

REVERSIBLE LOGIC ARITHMETIC UNIT

An Arithmetic Unit is a digital multifunctional circuit that performs Arithmetic (Sub, Add, Mul . . .) operations on two operands A and B. In today's world Arithmetic unit is very important part of any circuit or system and it have many applications in computers, cell phones, calculators and many more. The design of low delay, low power and high speed microprocessor must consume less power. The arithmetic circuit must be created using reversible logic gates so that power dissipation occurs because of information loss can be ignored. For the addition and subtraction operations we use DKG gate and for the multiplication and division operations we use Peres gate and NS gate

Logical unit

A Logical Unit is a digital circuit which performs logical (And, Or, Xor. . .) operations on two operands A and B. Arithmetic unit is very important part of any circuit or system and it have many applications in today's world The design of low delay, low power and high speed microprocessor must consume less power. This circuit must be created using reversible logic gates so that power dissipation occurs because of information loss can be ignored. For the various logic gates we use Peres gate, DKG gate, Feyman gate.

BASIC REVERSIBLE GATES

Design Verification is an important step in digital circuit design and often proves to the bottleneck in the IC development. Out of the different Design Verification areas, Functional Verification takes most of the time and effort.

Feyman Gate

The Controlled-Not gate commonly called the Feynman gate - is designed to produce the following output states: P = X and Q = X or Y. Since fanout is expressively forbidden in reversible logic, since a fanout has one input and two outputs, the Feynman gate can be used to duplicate a signal when Y is equal to 0.

Figure 01 Feyman Gate.

DKG Gate

A 4* 4 reversible DKG gate that can work singly as a reversible Full adder and a reversible Full subtractor.

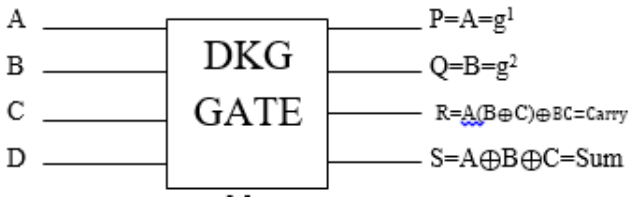
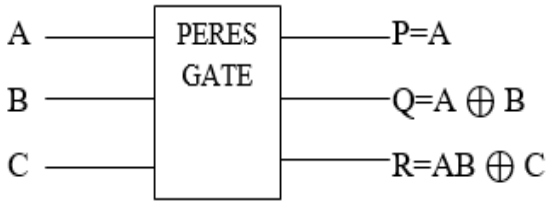


Figure 02 DKG Gate

It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. If input A=0, the proposed gate works as a reversible Full adder, and if input A=1, then it works as a reversible Full subtractor. It has been proved that a reversible full-adder circuit requires at least two garbage outputs to make the output combinations unique

Peres gate

The block diagram of Peres Gate in QCA is shown in Figure 1.3. Three of these, representing the inputs to the cell, are labeled A, B and C. Using the terminology of (Ma, X., 2008, Peres, A., 1985) the center cell is the "device cell" that performs the calculation. The remaining cell, labeled P, Q, and R provide outputs. The output is defined by P = A, Q = A ⊕ B and R=AB ⊕ C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.



N.S Gate

A 4 * 4 one through reversible gate called NS gate "NSG" is projected. The proposed reversible NSG gate is shown in Figure. . It can be established from the Truth Table that the input pattern analogous to a particular output pattern can be exclusively determined. The invented NSG gate can perceive all Boolean logical operators. The input d, c, b and a are termed as input terminal 1, 2, 3 and 4 respectively and the output are termed as output 1, output 2, output3 and output 4 respectively from first to last of the paper.

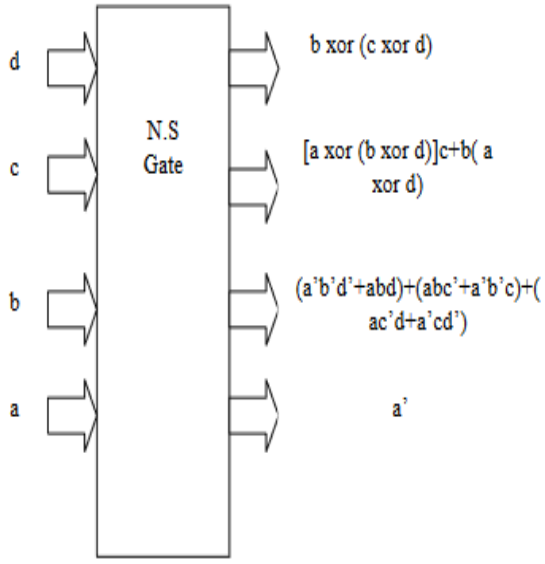


Figure 03 NS Gate

PROPOSED SYSTEM

A computer contains an arithmetic unit, a logical unit a control unit (CU) section a memory unit and input, output sections. Buses carry the information between these sections in the form of signals. They have a defined datapath. The ALU performs the arithmetic and logical operations. The control logic section retrieves instruction operation codes from memory, and initiates whatever sequence of operations of the ALU requires to carry out the instruction. A single operation code affects many individual datapaths, registers, and other elements of the processor.

Following steps are considered to design the desired reversible central processing unit (CPU):

- Design the whole structure of the CPU with reversible logic gates.
- Layout the datapath between all the components of the reversible CPU.
- Design the reversible flip-flops and realizing them
- Design the reversible memory circuits (such as buffer registers and counter circuits) using the proposed reversible flip-flops of the previous step.
- Design the arithmetic circuits such as adder, multiplier, divider, comparator etc.
- Design the reversible logical unit.
- Design the reversible control unit of the processor by designing an efficient instruction decoder.
- Construct the necessary logic to control the datapath.
- Realize the overall architecture and organization of the proposed reversible processor.
- Analysis of the proposed reversible central processing unit in terms of cost and performance efficiency.
- Simulate the design using Xilinx ISE design suite

A. Proposed Reversible Multiplexer

Reversible Multiplexer (Mux) is required to select a certain input from various input sources. A reversible 4-to-1 mux is designed with Fredkin gates. The proposed reversible 4-to-1 mux achieves the improvement of 57.14% in terms of number of gates, 54.54% in terms of garbage outputs, 73.68% in terms of quantum cost and 57.14% in terms of delay over the existing best one.

The architecture of the proposed reversible processor is shown in following figure.

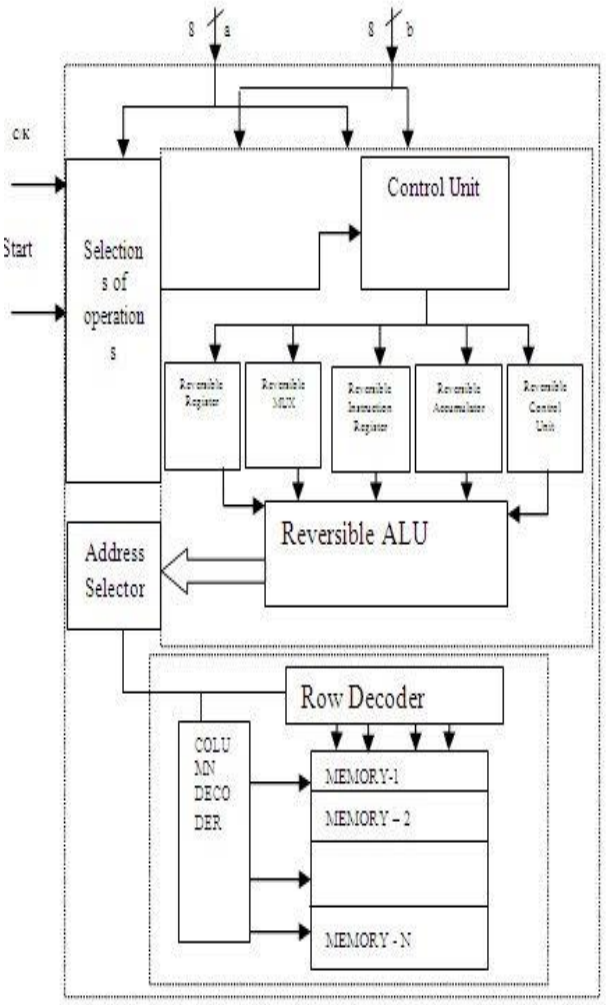


Figure 01 Proposed architecture of reversible CPU

B. Proposed Reversible Control Unit

A control unit is a circuit that directs operations within the computer's processor by directing the input and output of a computer system. The control unit consists of two decoders, a sequence counter, and a number of control logic gates. It fetches the instruction from instruction register. The inputs to the control logic gates come from two decoders, flip-flop and instruction register. The outputs of the control logic circuit are: signals to control the inputs of the registers, signals to control the read and write inputs of memory and signals to set, clear or complement the flip-flops.

A step by step design technique has been proposed to design the control unit which connects all the proposed components with some other extra circuitry. The block diagram of the proposed control unit is shown in following figure.

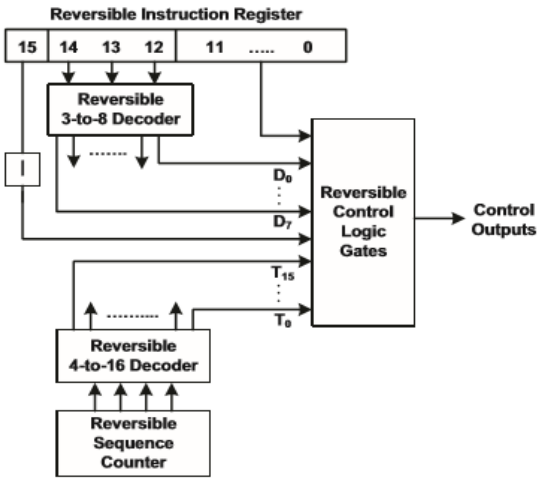


Figure 02 Reversible control unit

C. Proposed Reversible Adder

The proposed adder is built by using a reversible gate called DKG gate. The DKG gates are connected end to start to propagate the carry bit. The block diagram is shown as follows

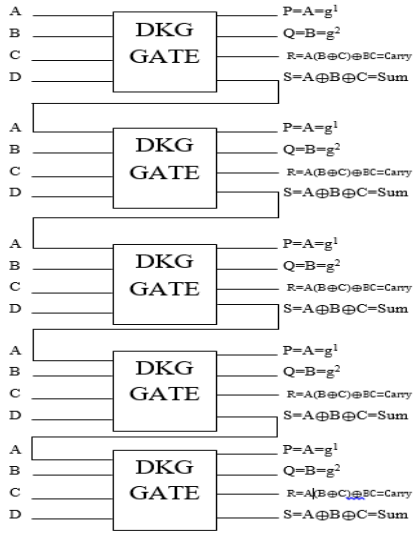
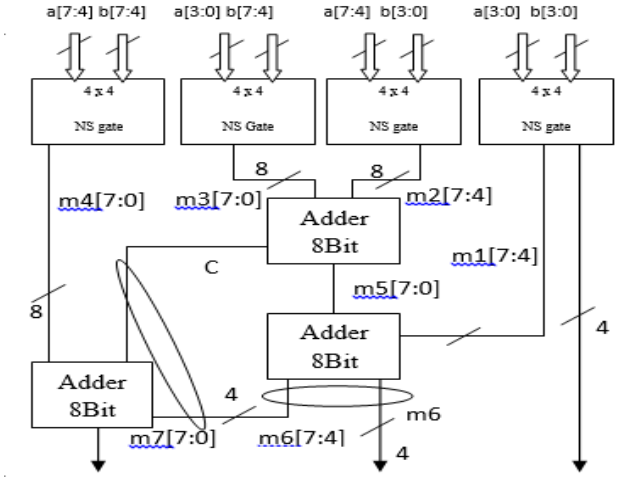


Figure 03 Proposed Reversible Gate

D. Proposed reversible Multiplier

The reversible adder circuits proposed till now, NS gate is better than the previous full adders design. The proposed full adder using NS Gate requires only one reversible gate (one NS Gate) and the NS Gate produces only 2 garbage outputs while performing operations like full adder, full subtractor, half adder and half subtractor. Apart from the other reversible gates proposed till now NS Gate can also singly perform the function of a full subtractor, half adder and half subtractor with only two garbage outputs now we design an multiplier.

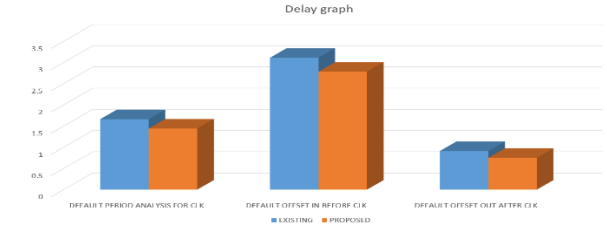


RESULT

1. TIMING ANALYSIS

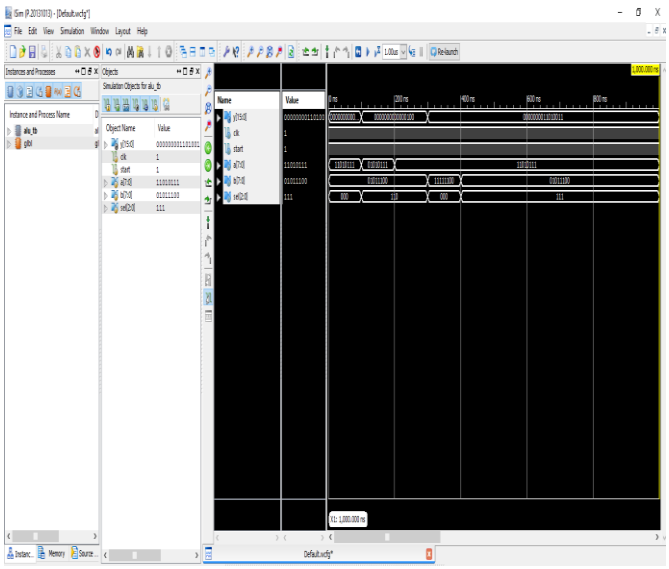
Timing analysis is done on xilinx planahead 14.4.

DELAY GRAPH SHEET



Simulation results

The following are the simulation results obtained for the reversible logic C.P.U.



CONCLUSION

In this work, reversible logic syntheses with the minimum cost factors are carried out for the components of the reversible processor. Many important contributions have been made in the literature towards the reversible implementations of arithmetic and logical structures. Multiplier is implemented in a different way using NS gate. A memory unit is designed with matrix forn of architecture with row and coloumn address. However, there have not been many efforts directed towards efficient approaches for designing reversible ALU (Arithmetic Logic Unit). Finally all the components of the reversible CPU (Central Processing Unit) will be interfaced together with necessary connecting circuits to get the complete reversible CPU. The proposed reversible CPU can make a significant contribution in the field of low power reversible computing and quantum computing.

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