An Efficient Architecture of MAC Unit with LAW Multiplier

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***Abstract:** In this paper, we propose an area and Delay efficient Multiply and Accumulate (MAC) unit using modified low area Wallace tree multiplier (LAW). Digital signal processing is the application of mathematical operations to digitally represented signals. MAC is the most important block in DSP system. High throughput multiplier accumulator (MAC) is always a key element to achieve a high-performance digital signal processing application for real time signal processing applications. This is because speed and throughput rate are always the concerns of digital signal processing systems. The key blocks of the MAC unit are multipliers and adders, in which multiplier is the one which occupies the major silicon area and consumes more power. In general, the multiplication operations are performed by the shift and add logic. Most of the DSP applications demand faster adders for its arithmetic computations. Carry Select Adder (CSLA) is a well known adder for its faster computation time. Recently, an efficient Carry Select Adder (CSLA) was proposed which significantly reduce the area and power by eliminating the redundant logic gates at each bit level. This is because the limited battery energy of these portable products restricts the power consumption of the system. The goal of this project is to design the VLSI implementation of MAC for high-speed DSP applications.*

Keywords— Multiply and Accumulate (MAC), LAW Multiplier, CSLA

I.INTRODUCTION

The MAC operation is the main computational kernel in Digital Signal Processing (DSP) architectures. The MAC unit is considered as one of the fundamental operations in DSP and it becomes a basic component in Application-Specific-Integrated-Circuits (ASIC). The MAC unit determines the speed of the overall system; it always lies in the critical path. Developing a high speed MAC is crucial for real time DSP applications.

Moreover, with the ever -increasing demand for WSN, a MAC unit with low power consumption would surely lead the market. Many researchers have attempted in designing MAC architectures with high computational performance and low power consumption. In order to improve the speed of the MAC unit, there are two major bottlenecks that need to be considered. The first one is the partial products reduction network that is used in the multiplication block and the second one is the accumulator. Both of these stages require the addition of large operands that involve long paths for carry propagation. Multiply - Accumulate is a common operation that computes the product of two numbers and adds that product to an accumulator. The multiplier A and multiplicand B are assumed to have n bits each and the addend Z has (2n+1) bits.

$$Z \leftarrow (A \times B) + Z$$

Multiplication is one of the most widely used arithmetic operations. Due to this a wide range of multiplier architectures are reported in the literature providing flexible choices for various applications. Among them the simplest is array multiplier [1] which is also the slowest. Some high performance multipliers are presented in [2–5]. The focus of this paper is Wallace multiplier [6]. Wallace multiplier uses full adders and half adders to reduce the partial product tree to two rows, and then a final adder is used to add these two rows of partial products. We call this design "TW (traditional Wallace) multiplier" in this text. TW multiplier performs its operation in three steps. (1) Generate all the partial products. (2)The partial product tree is reduced using full adders and half adders until it is reduced to two terms. (3) Finally, a fast adder is used to add these two terms.

Waters and Swartz lander [7] presented a reduced complexity Wallace multiplier by reducing the number of half adders in the reduction process. We call this design "RCW (reduced complexity Wallace) multiplier" from now on. The speed of the RCW multiplier is expected to be the same as of TW multiplier due to the equal number of reduction stages in both multipliers. The RCW uses a larger final adder as compared to the TW multiplier. A number of strategies are reported in [8] to improve the speed of the RCW. However, the focus of their research is to reduce the delay by using a faster final adder while still using the same reduction tree as RCW.As a result, the final adder size for the multipliers in [8] is the same as that of RCW. The focus of this paper is to optimize the reduction tree in a way that can reduce the size of the final adder. The reduced size of the final adder resulted in low area of the multiplier without incurring any extra delay.

II. PROPOSED 8X8 MAC UNIT DESIGN

Multiply Accumulate (MAC) unit consists of multiplier, adder and an accumulator. For high speed MAC unit, faster adder and multiplier circuits are required. The inputs for the Multiply Accumulate (MAC) unit are fetched from memory location and fed to multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location.

High throughput multiplier-and-accumulator is constantly an important factor to attain elevated performance digital signal processing applications in support of instantaneous applications of signal processing [9]. Since multiplier necessitates highest delay among fundamental operation

in digital system, significant path is limited by multiplier. Multiplier essentially consists of three functioning steps such as Multiplier, Adder and final Register shown in Fig 1. Multiplier- and-accumulator is essential element of digital signal as well as image/audio processing system for instance filtering, convolution as well as inner products consequently high speed is critical to expand for actual processing applications. Numerous researchers have attempted in scheming MAC for elevated computational performance as well as low power consumption. For high speed multiplication, Wallace tree multiplier is used, in which partial product is produced from Multiplicand (X) as well as Multiplier (Y).

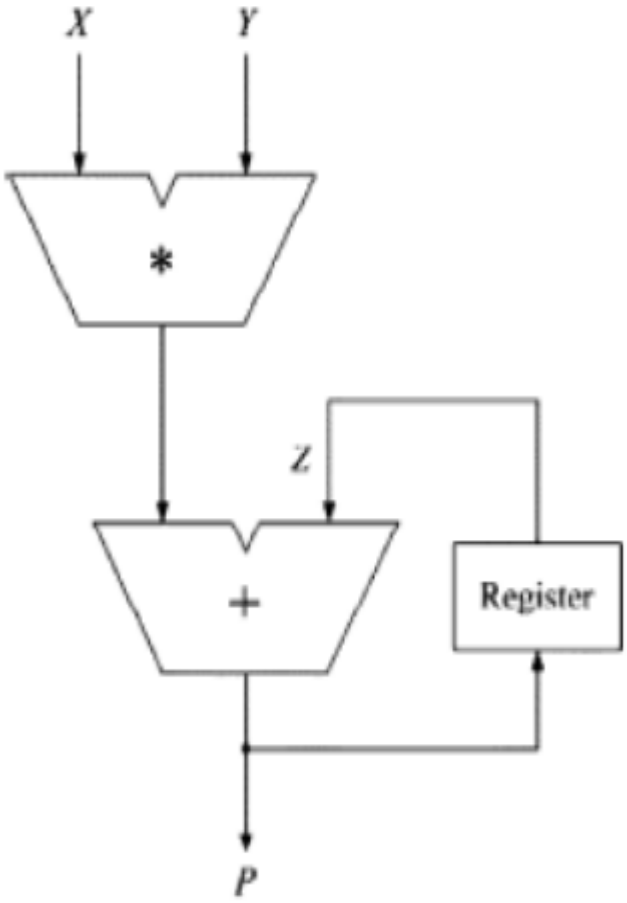

Fig 1 Overview of MAC unit

III.LOW AREA WALLACE TREE MULTIPLIER DESIGN

As discussed in the previous section, the critical path delay of the filter depends on the computation time of adder and multiplier. In this section, we have discussed an efficient architecture for adder and multiplier using modified carry select adder.

A. Wallace tree structure

In the past, several architectures have been proposed to perform the multiplication operations for serial as well as for parallel multipliers. In-that, the Wallace tree and Dadda multiplier are found to be faster than the conventional array multiplier [5] because its height is logarithmic in word size, not linear. The inputs to the Wallace tree is basically two unsigned integers.

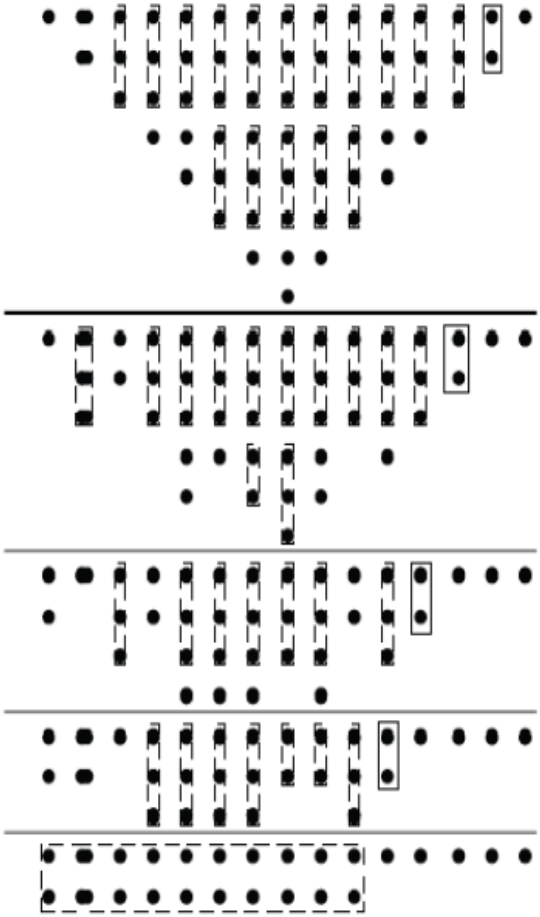

Fig 2 Architecture of Low Area Wallace Tree multiplier [10]

The Wallace tree requires large number of adder in each column to compute the summation of partial product bits. The designer's performed structural optimization in order to improve the latency of the total circuit. For our implementation, we have used the recently proposed Low Area Wallace (LAW) multiplier structure [10] rather conventional Wallace tree multiplier.

The partial products terms required for an N-bit multiplier are generated by using *N*2 AND gates. The dot notation is used to represent the partial product tree in all the architectures discussed in [10]. The full adders (FA) and half adders (HA) are represented by boxes around the dot products. The box which encloses three dot products represents a full adder, whereas the box containing only two dot products is used to represent a half adder. The stages are separated by a thick horizontal line. The architecture for 8-bit LAW multiplier is shown in Fig 2.

B. Modified Carry select adder

The conventional CSLA is not an area efficient one, as it requires two N-bit ripple carry adder blocks for pre-computation and a multiplexer to select the n-bit sum. To overcome the above mentioned issues, the authors [11] carried out the gate level optimization for a 1-bit CSLA structure by exploring the redundancy in the sum and carry generation Boolean expression. Hence, the need of EX-OR gate for generating the half sum in the conventional approach has been eliminated at each bit level. The Fig 3 shown below is the structure of1-bit modified carry select adder.

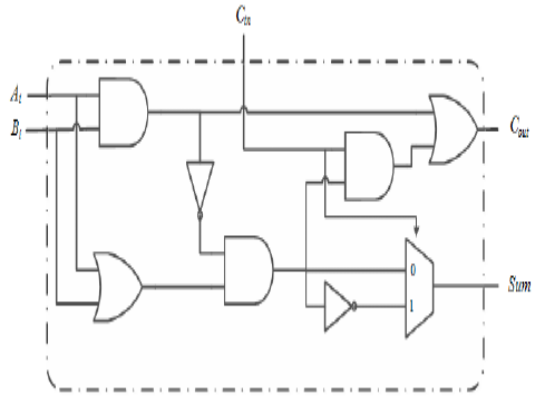

Fig 3 Architecture of 1-bit Modified Carry select adder [11]

The full adders and half adders in the Low Area Wallace multiplier structure are realized using the 1-bit CSLA module.

IV. SIMULATION RESULTS

The MAC unit simulated and synthesized using the Xilinx Design Suit13.2 with device family as spartan3E and device Xc3s100e-5vq100.

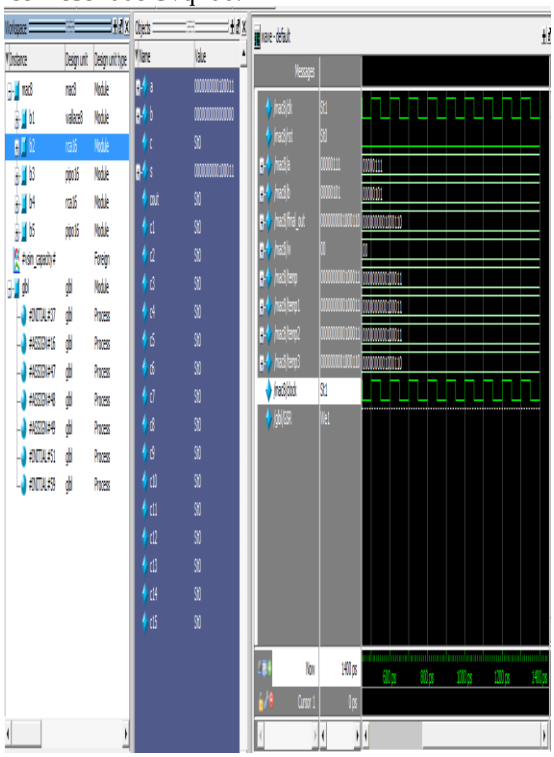

Fig 4 Simulation Results of 8-bit MAC unit

V.CONCLUSION

The time taken for multiplication operation is reduced by employing the Wallace multiplier. Here integrated reduced Wallace multiplier architecture is proposed for further reduction in time. In this project, the design of 8X8 bits MAC unit has been implemented using Wallace tree multiplier to reduce the area. This MAC unit has 16 bit output and its operation is to add repeatedly the multiplication results. All the basic blocks of MAC unit are identified and analyzed through its performance. The improvements achieved in low power consumption of the MAC unit can be used in high speed DSP applications.

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