Design An Advanced Encoder And Decoder By Using Odd And Even Inverts

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Abstract -In this paper, we perform a high-performance H-encoder/decoder with adaptive logic architecture for the VLSI implementation. By executing the coupling switching activity (C.S.A) obtained by different data encoding techniques (D.E.T). The proposed system called as Adavnced encoder and decoder (A.E.D) is introduced. The proposed encoding is inversion operation which is restricted to some encoding schemes. As the adaptive effective encoding technique gives better delay. The Xilinx 4.1 software is used for execution with Family SPARTAN 3E. The device and package used are XC3S100E and VQ100. Preferred verilog language to execute H-encoder/decoder with adaptive logic.

Key terms: A.E.D, C.S.A, D.E.T, Encoder, Decoder

I.INTRODUCTION

Encoder is a digital circuit that performs the inverse operation of decoder it has 2^n input lines and n output lines and it generates the binary code corresponding to the input values. Encoders are of two types they are incremental encoder (rotary/shaft encoder) and absolute encoder. Shafting encoder is an electro mechanical device which helps to convert the angular position or motion of a shaft or axle to an analog code or digital code.

It is a pulse generator that provides a square wave signals and a zero index[7]. To overcome this problem we gone through absolute encoder it has been developed to compensate for the performance and limitations of shaft It is a pulse generator that provides a square wave signals and a zero index. To overcome this problem we gone through absolute encoder it has been developed to compensate for the performance and limitations of shaft encoder this encoder must be reserved after a power interruption zero reset is help to obtain the mechanism angular position and sensitivity of interference[1].

This absolute encoder supplies the shaft position as a binary code. The output code is unique for each position
In this paper we focused on techniques aimed at adaptive encoding technique of power consumption by the Xilinx software here we use encoder and as well as decoder with the help of adders [4]. The proposed encoding schemes which are transparent with respect to the pulses implementation are presented and discussed at both binary/algorithmic level and the architectural level by means of simulation on synthesis and real traffic scenarios this result shows that by using the proposed encoding scheme up to 52% of power and 16% of energy can be saved without any significant degradation.

However, the encoding complexity of LDPC codes is still too high, which is a major problem that needs to be solved for their implementation. There have been some studies to reduce the encoding complexity using specially formed matrices such as a lower triangular matrix or semi-random matrix [6]. The encoding process of standard LDPC codes requires transferring a parity check matrix (H) into an equivalent systematic form, which can be accomplished by Gaussian elimination [6]. Gaussian elimination requires large memory and heavy calculation. The encoding process with a semirandom technique is much simpler than that using other matrices because it doesn't require Gaussian elimination [6]. Consequently, a linear time encoding is possible with very little memory. The hardware implementation of LDPC decoders is another problem to be considered when we use the fully parallel decoding algorithm of LDPC codes [8]. Although the fully parallel decoders can achieve a very high decoding speed, it is too complex to implement practically [6]. One of the best solutions for the decoder architecture is to directly instantiate the belief propagation (BP) algorithm in hardware [4]. In fully parallel decoding structures, all check nodes and variable nodes have their own processors and exchange messages between each check node and variable node at the same time.

In order to lower the hardware complexity, the number of check node and variable node processors needs to be reduced. In partly parallel decoding structures, part of variable nodes and check nodes perform the message passing process in time-division multiplexing mode. Therefore, there is trade-off between decoding throughput and hardware complexity in partly parallel structures. Although the hardware complexity of LDPC decoders is reduced using the partly parallel structures, these structures have a potential problem of encoding complexity because their parity check matrices may not be suitable for an efficient encoding process.

II. EXISTING STAGE SCHEME

Wireless mobile communication now demands large data bandwidth to accommodate various multimedia services. The third generation mobile communication, IMT-2000, provides 144 kbps for a fast moving terminal, 384 kbps for walking conditions, and 2 Mbps for stationary conditions [1]. The current bandwidth of IMT-2000 will not be enough to satisfy the various future demands for real-time and high quality service, compared to wired communication services for fast moving stations. The specification of fourth generation (4G) mobile communication is being developed to overcome the limitation. 4G mobile communication is supposed to provide 100 Mbps for a fast moving station and 155 Mbps to 1 Gbps for slow moving and stationary conditions. Such a system requires a very high speed wireless transmission technique.

A wireless channel environment is more subject

to noise than a wired channel because the signals are open to external disturbances such as path loss, shadowing, and fading. Therefore, channel coding is inevitable for wireless communication. Channel coding has been an important issue in communication systems. It has the ability to detect and correct errors caused by noise on a channel. The bit-error-rate (BER) can be reduced without increasing the signal power since the transmitted data carry redundancies that are used to detect and correct errors. This coding skill is useful in transmission on finite power channels such as general switched telephone networks [2]-[5]. To exist encoding technique I use encoder and decoder in scheme I focus on reducing the number of TYPE 1 and TYPE 2 transistors [1].

The scheme 1 compares the present data with previous one (flit) to decide whether the given input is odd inversion or no inversion of the present data can lead to power reduction if the previous bit is odd inverter before being transmitted, the dynamic power on the links are the self-transition activity of Types I, II, III and IV, respectively. For each transition the relationship between the coupling transition activities of the flit when transmitted as its bits are odd inverted. Here if the flit is odd inverted, Types II, III and IV transitions convert to the type I transitions. In case of transition types the type I transitions, the inversion of one of the Type II, III or Type IV transition respectively[1] SCHEME 2: Here I make use of both odd and full inversion the full inversion operation converts Type II to Type IV transition.

It compares the current data with the flit to decide whether the odd, full, or no inversion of the current data can give rise to the power reduction The power is dissipated when the flit is transmitted with no inversion, odd inversion and full inversion, respectively. The odd inversion lead to power reduction and the full inversion satisfied inequality. The operating principles of this encoder are similar to the previous encoder. Here again the previously encoded body flit is indicated with inv which defines if it was odd or full inverted (inv=1) or left as it was (inv=0).

In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales [5]. In particular, we present a set of data encoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both the switching activity and the coupling switching activity on links of the routing paths traversed by the packets. The proposed encoding schemes, which are transparent with respect to the router implementation, are presented and discussed at both the algorithmic level and the architectural level, and assessed by means of simulation on synthetic and real traffic scenarios.

The analysis takes into account several aspects and metrics of the design, including silicon area, power dissipation, and energy consumption. The results show that by using the proposed encoding schemes up to 51% of power and up to 14% of energy can be saved without any significant degradation in performance and with 15% area overhead in the NI.

III. PROPOSED SYSTEM

H-Encoder It is better codes of error controlling performance. H-Encoder outputs are not only associated with the encode elements at present, but also affected by several ones before. Data 1 and data 2 are used for describing codes, where data 1 are the input encode elements, data out is the output encode elements and data 2 is the shift register number of encoder Data 1 and Data 2 are the inputs of the Encoder. Their architecture design with chip registers perform their operations and gives output of the encoder is Data out as shown in fig 1.

H-Decoder Two parallel binary bits are inputted into the H-decoder with every clock pulse, and then it begins to work when the input enabling signal is valid. Each group consists of two because each current state can be reached by decoder path. Here Data out is the output of the encoder similarly Data out and Data 2' are the inputs of Decoder. These inputs will perform as per their chip architecture design and the output of the decoder is Data as shown in fig-1.

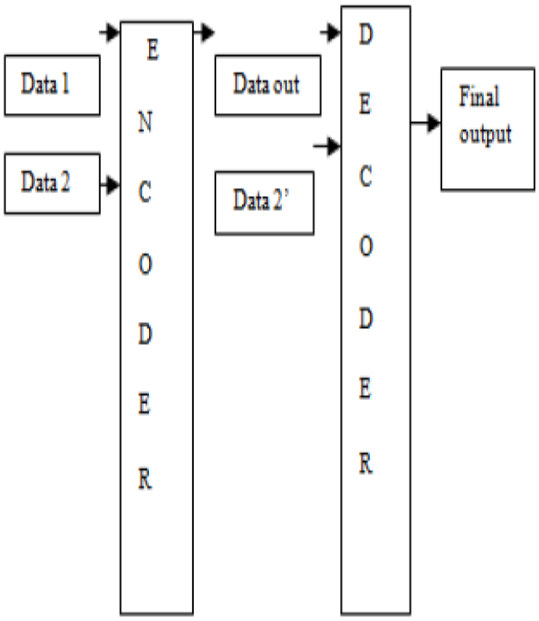

Fig.1.H-Encoder/Decoder with Adaptive Logic

Figure 1 indicates the block diagram of H-encoder/decoder with adaptive logic. The H-encoder/decoder with adaptive logic consists of four shift registers and two exclusive-or gates. Every shift register is equivalent to a flip flop. These four flip flops are connected in series to complete shifting and updating operation under the action of the clock pulse. The exclusive-or gates are used for inner operation of coding data. With every clock pulse the encoder outputs two bits according to the generator polynomials whenever one binary bit is inputted. The output is not only relevant with the current input binary bit, but also influenced by the previous bit for decoder.

TECHNICAL SCHEMATIC:

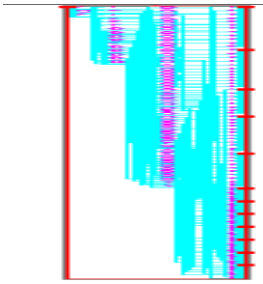

FIG.2.Technical Schematic

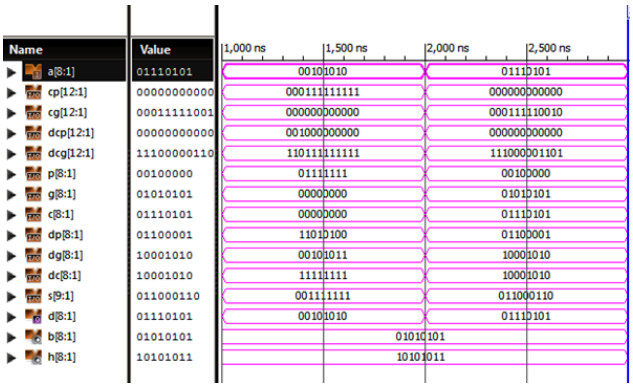

FIG.3.Output Waveforms

OUTPUT WAVEFORMS

Fig-3 shows the output waveforms of data adaptive encoding techniques. Here we have given a[8:1] as a input data for encoder and s[9:1] taken as output for encoder. As well as s[9:1] taken as input data for decoder where as d[8:1] is the output for decoder.

The H-Encoder/Decoder with Adaptive logic decides the proposed algorithm to work with adaptive logic. The registers are work with the adaptive techniques, by using this technique, the proposed algorithm increases the speed i.e. decrease the delay.

CONCLUSION

A.E.D is based on the proposition that Genetic algorithm finds good solutions to a problem. Studying the existing encoding schemes I, II & III is proposed. The A.E.E.S encoding scheme. The proposed encoding supports one point crossover as in binary encoding and A.E.D crossover as in encoding. The proposed encoding is inversion operation which is restricted to some encoding schemes. A.E.D is very efficient in speed. As the adaptive effective encoding technique gives better delay. By using proposed system we can reduce delay by 17.38ns to 10.46ns

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