Hybrid System (Solar+Wind) Based Distributed Generation With QUASI –Z-SOURCE Inverter

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Abstract - The voltage-fed Z-source inverter/quasi-Z-source inverter (qZSI) has been presented suitable for photovoltaic (PV) applications mainly because of its single-stage buck and boost capability and improved reliability. This paper further addresses detailed modeling and control issues of the qZSI used for distributed generation (DG), such as PV or fuel cell power conditioning. The dynamical characteristics of the qZSI network are first investigated by small-signal analysis. Based on the dynamic model, stand-alone operation and grid-connected operation with closed-loop control methods are carried out, which are the two necessary operation modes of DG in distributed power grids. Due to the mutual limitation between the modulation index and shoot-through duty ratio of qZSI, constant capacitor voltage control method is proposed in a two-stage control manner. Minimum switching stress on devices can be achieved by choosing a proper capacitor voltage reference. Experimental results are presented for validation of the theoretical analysis and controller design.

Index Terms—DC–AC converter, distributed generation (DG), quasi-Z-source inverter (qZSI), renewable energy source (RES).

I. INTRODUCTION

Photovoltaic (PV) power generation is becoming more promising since the introduction of the thin film PV technology due to its lower cost, excellent high temperature performance, low weight, flexibility, and glass-free easy installation [1]. However, there are still two primary factors limiting the widespread application of PV power systems. The first is the cost of the solar cell/module and the interface converter system; the second is the variability of the output of the PV cells. A PV cell's voltage varies widely with temperature and irradiation, but the traditional voltage source inverter (VSI) cannot deal with this wide range without over rating of the inverter, because the VSI is a buck converter whose input dc voltage must be greater than the peak ac output voltage [2]-[3]. A transformer and a dc/dc converter is usually used in PV applications, in order to cope with the range of the PV voltage , reduce inverter ratings, and produce a desired voltage for the load or connection to the utility.

In Recent Years, wind energy has been regarded as one of the significant renewable energy sources [4]. Among the existing wind power generation systems, their generators can be categorized into four main types: 1) fixed-speed squirrel-cage induction generator, 2) variable-speed wound rotor induction generator that employs variable rotor resistance, 3) variable-speed doubly fed induction generator that employs a frequency converter between the grid and its rotor windings and 4) variable-speed synchronous generator, which is either a wound rotor synchronous generator or a permanent-magnet synchronous generator (PMSG). Due to the fact that a multiple pole design can be easily realized in the synchronous generator, it is the only type that provides a realistic opportunity to implement gearless operation and hence, the features of lightweight and low maintenance can be obtained in wind generation system [5]-[6].

More efforts are now being put into distributed power generation of renewable energy sources (RESs), such as photovoltaic (PV), wind power, and fuel cells, which are sustainable and environmental friendly. Practically, several distributed generations (DGs) consist of distributed power grid and further construct microgrid with local loads and managements. To ensure proper performance of the microgrid, DG is usually required to work in two modes: stand-alone or grid connected.

As an interface between RES and distributed power grid, the performance of power electronic converters becomes critical. Z-source inverter (ZSI) is known as a single-stage buck/boost inverter [1]. With an impedance network coupling the inverter main circuit to the dc source, the ZSI achieves voltage buck/boost in one stage, without introducing more switching devices. Shoot-through state enables energy to be stored in

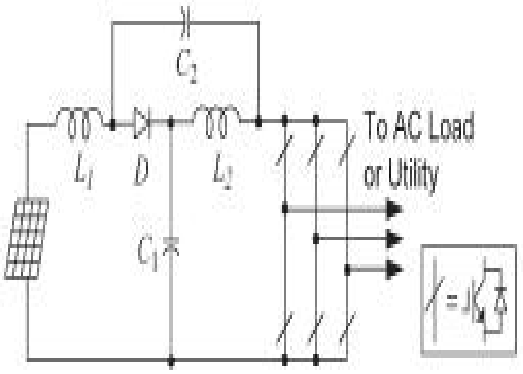


Fig. 1. Voltage-fed qZSI with continuous input current for PV application.

Inductors, which is released when at non-shoot-through state, followed by the voltage boost feature. For the voltage-fed type ZSI (abbreviated as ZSI), voltage boost methods based on pulsewidth modulation (PWM) have been first investigated as simple boost control, maximum boost control, and maximum constant boost control [1]–[3]. Because of its single-stage voltage buck/boost properties, the ZSI can deal with input voltage fluctuation in a wide range, which is conventionally achieved by a two-stage dc–dc converter cascaded by dc–ac structure [4]–[6]. With the economical advantages and improved reliability due to the allowance of shoot-through state, ZSI gains increasing attention and was presented for use in several applications, such as DG, uninterruptible power system, fuel cell vehicles, PV or wind power conversion, and electronic loads [7]–[15]. Design guidelines of the impedance network are analyzed in terms of both steady-state and dynamic performances [16], [17]. By applying

state-space averaging, the dynamic modeling and transient analysis of the Z-source network are investigated [18], [19]. Closed-loop controller is developed for ZSI control [7], [20]–[22]. The dependence of control variables *d*0 (shoot-through duty ratio) and *M* (modulation index) of the ZSI is taken into consideration [21], [22]. Moreover, the discontinuous conduction mode of the ZSI with small inductance or low load power factor and its associated circuit characteristics are analyzed in [23].

With a set of new topologies of the impedance networks, a class of quasi-Z-source inverter (qZSI) has been derived from the original ZSI and applied to DG applications [24]–[26]. A voltage-fed qZSI (shown in Fig. 1) was proposed in [25] for PV applications because of continuous input current and reduced passive component (capacitor) rating—capacitor voltage on *C*2 is much less than that on *C*1 during operating and this feature leads to lower manufacture cost. This paper further investigates the detailed modeling and control issues of the qZSI to be applied in DG applications. The dynamic model of the asymmetric quasi-Z-source network is constructed by small-signal analysis. System characteristics are carefully investigated in terms of component parameter and system

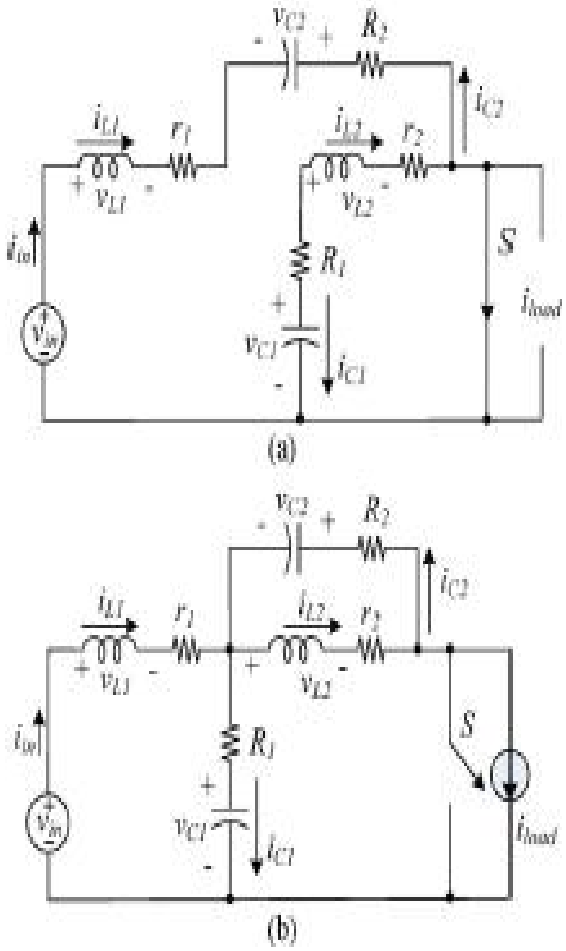


Fig. 2. Equivalent circuit of quasi-Z-source network when in the (a) shoot through and (b) non-shoot-through states.

operating condition. Based on the dynamic model, a two-stage control method is proposed with detailed design concerns. Constant capacitor voltage is maintained to avoid the overlap of *d*0 and *M* throughout the whole operating condition. With the proposed control strategy, qZSI shows promising application future to couple the RES that features a wide voltage variation range to a distributed power grid.

II. LITERATURE SURVEY

A single-phase square wave type voltage source inverter produces square shaped output voltage for a single-phase load. Such inverters have very simple control logic and the power switches need to operate at much lower frequencies compared to switches in some other types of inverters, discussed in later lessons. The first generation inverters, using thyristor switches, were almost invariably square wave inverters because thyristor switches could be switched on and off only a few hundred times in a second. In contrast, the present day switches like IGBTs are much faster and used at switching frequencies of several kilohertz. As pointed out in Lesson-26, single-phase inverters mostly use half bridge or full bridge topologies. Power circuits of these topologies are redrawn in Figs. 34.1(a) and 34.1(b) for further discussions.

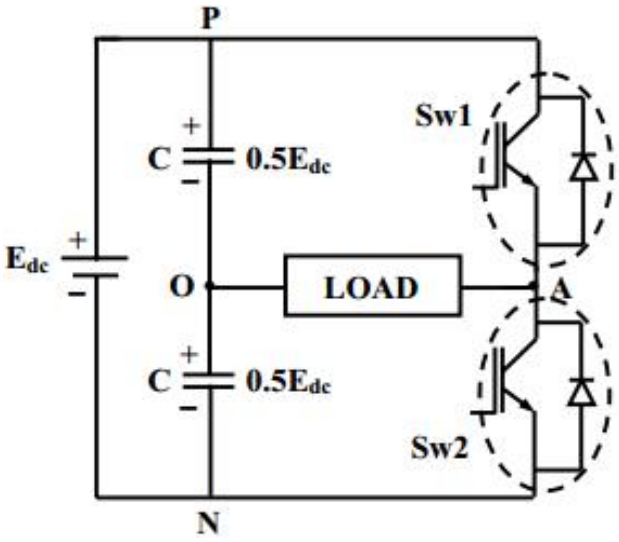


Fig. (a): A 1-phase half bridge VSI

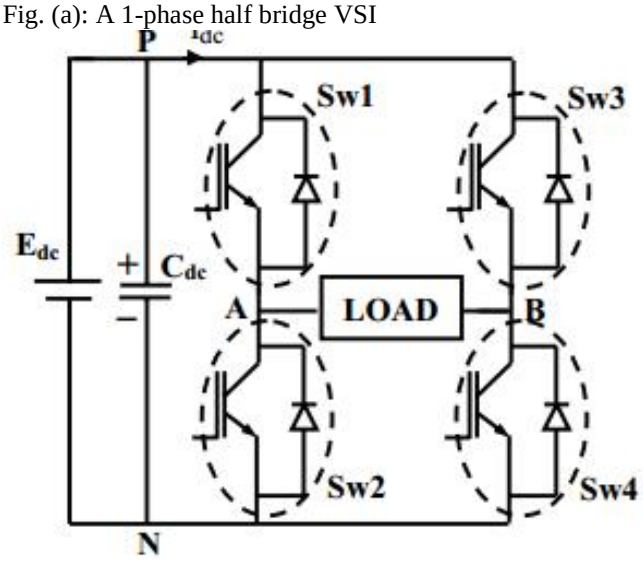


Fig. (b): A 1-phase full-bridge VSI

In this lesson, both the above topologies are analyzed under the assumption of ideal circuit conditions. Accordingly, it is assumed that the input dc voltage (E_{dc}) is constant and the switches are lossless. In half bridge

topology the input dc voltage is split in two equal parts through an ideal and loss-less capacitive potential divider. The half bridge topology consists of one leg (one pole) of switches whereas the full bridge topology has two such legs. Each leg of the inverter consists of two series connected electronic switches shown within dotted lines in the figures. Each of these switches consists of an IGBT type controlled switch across which an uncontrolled diode is put in anti-parallel manner. These switches are capable of conducting bi-directional current but they need to block only one polarity of voltage. The junction point of the switches in each leg of the inverter serves as one output point for the load.

In half bridge topology the single-phase load is connected between the mid-point of the input dc supply and the junction point of the two switches (in Fig. 34.1(a) these points are marked as 'O' and 'A' respectively). For ease of understanding, the switches Sw1 and Sw2 may be assumed to be controlled mechanical switches that open and close in response to the switch control signal. In fact in lesson-33 (section 33.2) it has been shown that the actual electronic switches mimic the function of the mechanical switches. Now, if the switches Sw1 and Sw2 are turned on alternately with duty ratio of each switch kept equal to 0.5, the load voltage (V_{AO}) will be square wave with a peak-to-peak magnitude equal to input dc voltage (E_{dc}). Fig. 34.2(a) shows a typical load voltage waveform output by the half bridge inverter. V_{AO} acquires a magnitude of +0.5 E_{dc} when Sw1 is on and the magnitude reverses to -0.5 E_{dc} when Sw2 is turned on. Fig. 24.2 also shows the fundamental frequency component of the square wave voltage, its peak-to-peak magnitude being equal to $4/\pi\ E_{dc}$. The two switches of the inverter leg are turned on in a complementary manner. For a general load, the switches should neither be simultaneously on nor be simultaneously off. Simultaneous turn-on of both the switches will amount to short circuit across the dc bus and will cause the switch currents to rise rapidly. For an inductive load, containing an inductance in series, one of the switches must always conduct to maintain continuity of load current. In Lesson-33 (section 33.2) a case of inductive load has been considered and it has been shown that the load current may not change abruptly even though the switching frequency is very high. Such a situation, as explained in lesson-33, demands that the switches must have bi-directional current carrying capability.

III. PROPOSED METHOD AND RESULTS

Small-Signal Model of the Quasi-Z-Source Network

By applying a two-stage control strategy to be presented later on, the control of dc side and that of ac side are decoupled. With an intention to provide a comprehensive mathematical guide in terms of the qZSI dc-side modeling, small-signal analysis is used for the studies, along with detailed derivations.

For general analysis purposes, input voltage *v*in is chosen as system input, to which input current *i*in is related. This is because RES does not have as stiff output characteristics as an ideal voltage source or current source. The relationship of *v*in and *i*in will be determined by specified energy source nature. For dc-side modeling, the three-phase inverter bridge and external ac load are represented by a single switch and a current source connected in parallel [17], [19]. As previously mentioned, when operating at shoot-through states, the ac load terminals are shorted through both upper and lower devices of any phase leg(s); therefore, the single switch is ON, and the equivalent circuit of the qZSI is shown in Fig. 2(a). When operating at non-shoot-through states (i.e., six active states and two conventional zero states where either all the upper devices or all the lower devices are gated on), the single switch is OFF, and the equivalent circuit of the qZSI is shown in Fig. 2(b).

Considering the asymmetric quasi-Z-source network, there are four state variables: the currents through two inductors *iL*1 and *iL*2 and the voltages across the capacitors *vC*1 and *vC*2. Independent load current *i*load serves as another input (disturbance) of the quasi-Z-source network. Choose *vC*1 and *iL*1 (= *i*in) as the output of the studied system. For simplification, assume that $C = C1 = C2$, $L = L1 = L2$, the stray resistances of inductors $r = r1 = r2$, and the equivalent series resistances of capacitors $R = R1 = R2$. Define shoot-through interval $T0$, non-shoot through interval $T1$, and switching period $Ts = T0 + T1$; thus, the shoot-through duty ratio is $d0 = T0/Ts$.

At the shoot-through state shown in Fig. 2(a), the capacitors transfer their electrostatic energy to magnetic energy stored in the inductors. The dynamic state equations of the quasi-Z source network are given as

$$\frac{d\mathbf{x}}{dt} = \mathbf{A_1 x} + \mathbf{B_1 u} \qquad (1)$$

where

$$\mathbf{x} = [i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}]'$$

$$\mathbf{A_1} = \begin{bmatrix} -((r+R)/L) & 0 & 0 & 1/L \\ 0 & -((r+R)/L) & 1/L & 0 \\ 0 & -(1/C) & 0 & 0 \\ -(1/C) & 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{B_1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1/L & 0 & 0 & 0 \end{bmatrix}'$$

$$\mathbf{u} = [i_{\text{load}}\ v_{\text{in}}]'.$$

At the non-shoot-through states shown in Fig. 2(b), the dc power source, as well as the inductors, charges the capacitors and powers the external ac load, boosting the dc voltage across the inverter bridge. The dynamic state equations are shown as

$$\frac{d\mathbf{x}}{dt} = \mathbf{A_2 x} + \mathbf{B_2 u} \qquad (2)$$

where

$$\mathbf{A_2} = \begin{bmatrix} \frac{-(r+R)}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{(r+R)}{L} & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix}$$

$$\mathbf{B_2} = \begin{bmatrix} \frac{R}{L} & \frac{1}{L} \\ \frac{R}{L} & 0 \\ -1/C & 0 \\ -1/C & 0 \end{bmatrix}.$$

Using state-space averaging, the dc-side model of qZSI can be obtained as shown in

$$\frac{d\mathbf{x}}{dt} = \mathbf{Ax} + \mathbf{Bu} \qquad \mathbf{y} = \mathbf{Cx} + \mathbf{Du} \tag{3}$$

where

$$\mathbf{A} = d_0\mathbf{A}_1 + (1-d_0)\mathbf{A}_2,\ \mathbf{B} = d_0\mathbf{B}_1 + (1-d_0)\mathbf{B}_2,$$
$$\mathbf{y} = \begin{bmatrix} v_{C1} \\ i_{L1} \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}, \text{and } \mathbf{D} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

To obtain the small-signal model, perturbations ˆ *d*0, ˆ*v*in, and ˆ*I* load are introduced with *d*0, *v*in, and *i*load, respectively, which, in turn, cause variations ˆ*iL*1, ˆ*iL*2, ˆ*vC*1, and ˆ*vC*2 in the dynamic state variables of *iL*1, *iL*2, *vC*1, and *vC*2. Substituting *x* = *X* + ˆ*x* (where *X* and ˆ*x* are the dc terms and perturbations of the variables *x* = *d*0, *v*in, *i*load, *iL*1, *iL*2, *vC*1, and *vC*2) into (3), considering the principles of inductor volt–second

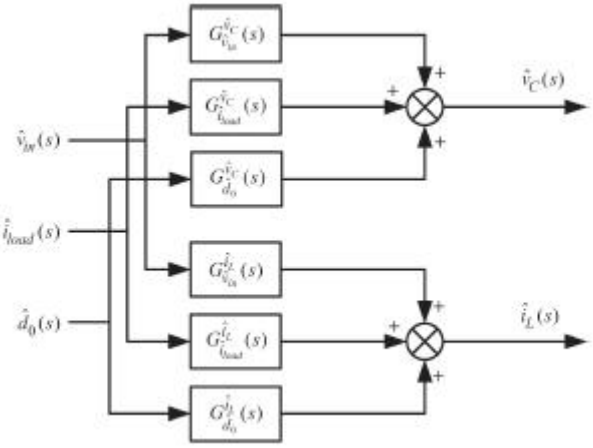


Fig. 3. Small-signal model of the quasi-Z-source network.

And capacitor charge balance in steady state, and ignoring the second-order elements, the Laplace-transformed transfer functions of the multi-input multioutput quasi-Z-source network can be derived. The small-signal model of the quasi-Z-source network is shown in Fig. 3. Assuming any two of the system inputs to be zero, one can get small-signal transfer functions from the remaining to the state variables.

7.2 Dynamic Characteristics of the Quasi-Z-Source Network

According to the small-signal model, the transfer functions from *d*0 to capacitor voltages *vC*1 and *vC*2 are identical, denoted as *G*ˆ*vC* ˆ *d*0 (*s*) in (4), shown at the bottom of the page. Other transfer functions are given in the Appendix.

Based on these equations, the characteristic equation of the quasi-Z-source network can be obtained as

$$G_{d_0}^{\hat{v}_C}(s) = \left.\frac{\hat{v}_C(s)}{\hat{d}_0(s)}\right|_{\substack{\hat{i}_{load}(s)=0 \\ \hat{v}_{in}(s)=0}}$$
$$= \frac{(V_{C1}+V_{C2}-RI_{load})(1-2D_0)+(I_{load}-I_{L1}-I_{l2})(Ls+r+R)}{LCs^2+C(r+R)s+(1-2D_0)^2}$$

(4)

$$s^2 + \frac{r+R}{L}s + \frac{(1-2D_0)^2}{LC} = 0. \tag{5}$$

Equation (5) can be written as the following normalized form:

*s*2 + 2*ξωns* + *ω*2*n* = 0 (6)

Where

$$\omega_n = \frac{1-2D_0}{\sqrt{LC}}$$

Is the natural frequency and

$$\xi = \frac{r+R}{2(1-2D_0)}\sqrt{\frac{C}{L}}$$

Is the damping ratio. Among these equations, *D*0, *I*load, *VC*1, *VC2*, *IL*1, and *IL*2 represent a given equilibrium point nearby where the system can be literalized. Equation (5) indicates that, aside from the parameters of the quasi-Z-source network (i.e., *L*, *C*, *r*, and *R*), *D*0 is also one factor to determine the system dynamic characteristics.

To make a clear map of the dynamic characteristics of the quasi-Z-source network, various root loci of the transfer function *G*ˆ*vC*ˆ *d*0 (*s*) are studied by parameter sweep of *L*, *C*, and *D*0.

The system specifications are as follows: *L* = 500 *μ*H, *C* = 400 *μ*F, *R* = 0.03 Ω, *r* = 0.47 Ω, *D*0 = 0.25, *I*load = 9.9 A, and *V*in = 130 V. Fig. 4 shows the pole and zero trajectories of *G*ˆ*vC* ˆ *d*0 (*s*) with *L*, *C*, and *D*0 variations, respectively. The quasi-Z-source network exhibits similar characteristics as the Z-source network studied in [17]–[19]. There is a right-half plane (RHP) zero in *G*ˆ*vC*ˆ *d*0(*s*), which is learned to imply high gain instability and impose control limitations. A feedback should be carefully designed with an adequate phase margin. It can be observed from Fig. 4(a) that, along with increasing *L*, zeros are pushed from the right half-plane toward the origin along the real axis, indicating an increasing degree of non minimum-phase undershoot (e.g., capacitor voltage dips before it rises in response to *d*0 rising). Similar conclusion can be reached with an increase in *D*0 from Fig. 4(c). However, the variation of *C* has very little influences on the RHP zeros seen from Fig. 4(b).

Additionally, the conjugated pole pairs are observed to move toward the origin along with the increase in *L*, as shown in Fig. 4(a). The feedback control performance is predicted deteriorated with the increase in *L*. Moreover, increasing in *L* causes smaller damping ratio

and decreasing natural frequency, which is consistent with (6). On the other side, the conjugated pole pairs can be seen shifting toward the real axis with the increase in *D*0 or *C*, implying increasing system settling time and decreasing natural frequency, which is consistent with (6) too. The placement of poles and zeros gives an important guideline for passive component selection of qZSI design: Although large *L* and *C* are preferred for low steady-state current and voltage ripples, tradeoffs need to be made for proper transient responses.

8. CAPACITOR VOLTAGE CONTROL

It is learned from literatures that, to increase voltage gain of the qZSI, one can increase either the shoot-through duty ratio *d*0 or the modulation index*M*. However, due to its single-stage structure, *d*0 and *M* are dependent on each other. This can be explained by that the voltage boost of qZSI is achieved by partly

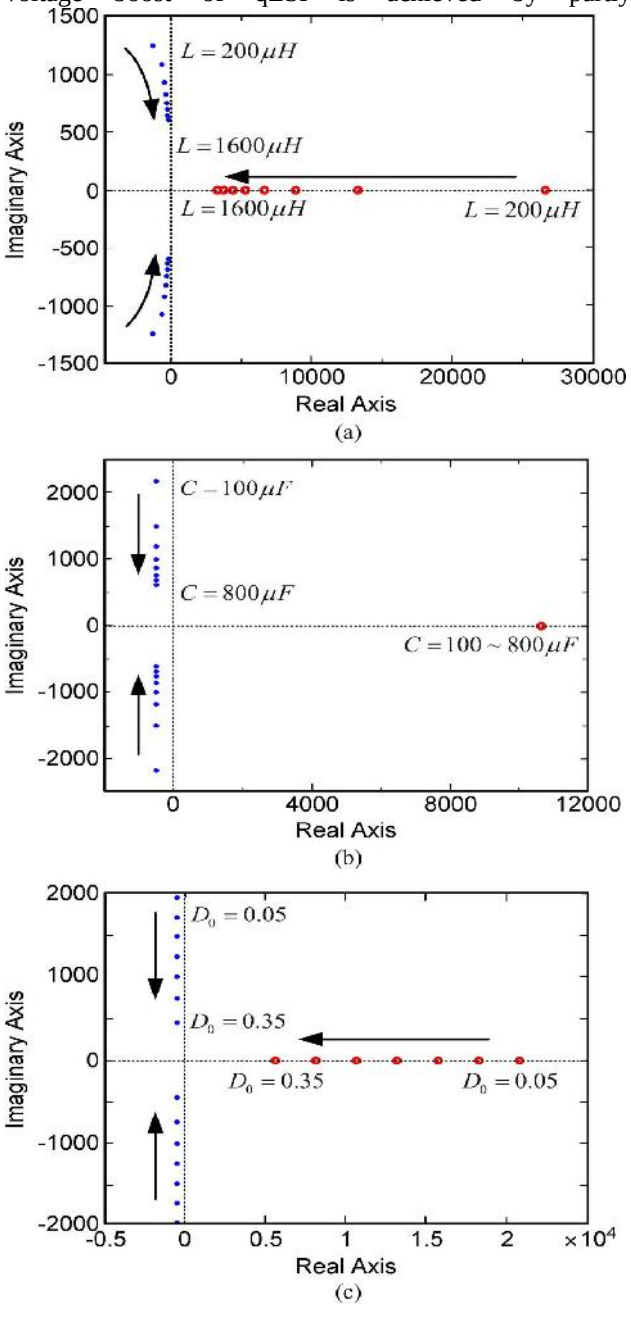


Fig. 4. Pole–zero map of transfer function *GˆvC ˆ d*0 (*s*), with parameter sweep of (a) *L*, (b) *C*, and (c) *D*0.

Or fully replacing conventional zero states (000 or 111) with shoot-through state, leaving six active states unchangeable [1] (which is associated with *M*). Thus, (7), (8), or (9) has to be yielded according to the boost method engaged [1]–[3] simple boost:

$M \le 1 - D0$ (7)

Maximum constant boost: $M \le \sqrt{2}/3\ (1 - D0)$ (8)

Maximum boost: $M \le 2\pi/3\sqrt{3}.(1 - D0)$. (9)

Symbol*D*0 is used to imply a steady state. As a result, changing either *d*0 or *M* will impose a limitation on the other parameter, which makes it become challenging to design the controller.

On the other hand, to use a large *d*0 but a small*M* for the same voltage gain is not cost effective, because this increases voltage stress across devices [25], which results in high component rating.

Notice that, in steady state, the peak phase voltage of the inverter can be written as

$$v_{p\_peak} = \frac{1}{2} \cdot \frac{V_{in}}{1 - 2D_0} \cdot M. \quad (10)$$

As described in [24], the relationship between the capacitor voltage and the input voltage can be expressed as

$$V_{C1} = \frac{1 - D_0}{1 - 2D_0} V_{in}. \quad (11)$$

Dividing (11) by (10) results in

$$\frac{V_{C1}}{v_{p\_peak}} = \frac{2(1 - D_0)}{M}. \quad (12)$$

Referring to (7)–(9), the capacitor voltage inequality can be derived as

simple boost: $VC1 \ge 2vp`peak$ (13)

Maximum constant boost: $VC1 \ge 3\sqrt{3}vp`peak$

$\approx 1.73vp`peak$ (14)

Maximum boost: $VC1 \ge 3\sqrt{3}\pi / vp`peak$

$\approx 1.65vp`peak$ (15)

Equations (13)–(15) imply that, to avoid overlap of *d*0 and *M*, one can simply keep voltage on *C*1 above twice the output peak voltage at the most. Since *vp*`peak is fixed in most DG applications, it is possible to control the capacitor voltage in a constant value with input variation. In a closed-loop control, one can keep a minimum capacitor voltage referring to (13)–(15); then, the minimum *D*0 and the maximum *M* can be inherently achieved, which lead to the lowest voltage stress across devices.

For DG applications, the qZSI is expected to be able to work in both stand-alone and grid-connected modes. To operate in stand-alone mode, DGs in parallel usually construct the distributed power grid in a master–slave manner or all serve as virtual synchronous generators. Thus, the master qZSI or all qZSIs in parallel need to follow a voltage reference to maintain local power balance and valid system voltage and frequency.

To operate in grid-connected mode or serve as the slave DG in stand-alone mode, since the output voltage is arbitrarily given by the utility or master DG, the qZSI should follow a current reference to control the output active and reactive power. To an end, the controlled qZSI turns out two essentially different output characteristics: a voltage source or a current source. The next section will discuss the controller design for both types, respectively. Transition between the two operating modes for DG applications can be made on the microgrid level, where power rebalance and resynchronization are the most concerned aspects. With system reconfiguration by break actions and necessary protections, qZSIs can make transition between

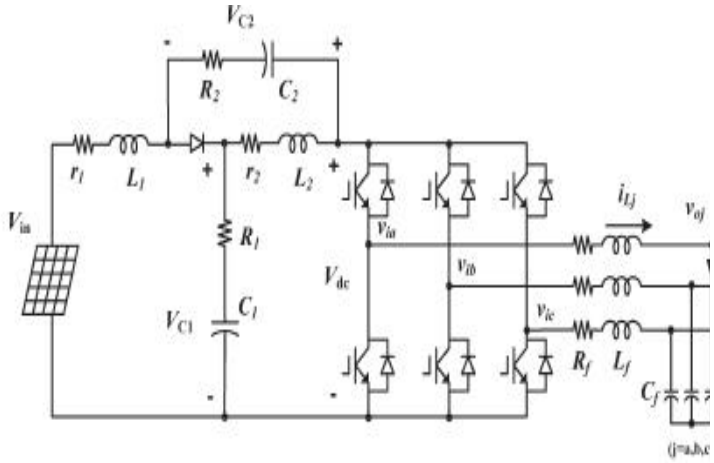


Fig. 5. System configuration of the proposed qZSI for DG applications.

Voltage control and current control with precise output power management, relying on modern communication approaches, such as power line or wireless communication.

9. TWO-STAGE CONTROL METHODOLOGY FOR QZSI-BASED DG

Fig. 5 shows the overall system configuration of the proposed qZSI, where *Lf* , *Rf* , and *Cf* are the inductance, capacitance, and stray resistance of the filter, respectively, and *voj*, *iCj*, *vij*, *iLj*, *ioj* , and *igj* are the load voltage, capacitor current of the filter, output voltage of the inverter, inductor current of the filter, load current, and grid current, respectively, all in three phases (*j* = *a*, *b*, *c*). CB stands for circuit breaker.

CB1 is ON and CB2 is OFF when the qZSI works under voltage control mode, and CB1 is OFF and CB2 is ON when the qZSI is under current control mode. It should be pointed out that, although one qZSI with variable resistive load is used to demonstrate the voltage control strategy, the controller design principle is still applicable to qZSIs that are connected in parallel.

9.1. Controller Design for Output Voltage Control

Through the decoupling capacitor, control of dc side and that of ac side are executed separately, as shown in Fig. 6. Pulses generated by the dc-side controller (for voltage boost) and the ac-side controller (for dc–ac conversion) are combined together by logical OR to fire six insulated-gate bipolar transistors, assuming "1" is ON and "0" is OFF. The overlap of *d*0 and *M* can be avoided by setting the reference of the capacitor

voltage *vC*1 based on (13)–(15), depending on the different boost control methods involved.

For the dc-side control, capacitor voltage *vC*1 is measured and fed back. The dynamics of *vC*1 caused by *d*0 can be obtained via transfer function *G*ˆ*vC* ˆ *d*0(*s*), as shown in (4). Linear approximation of the RES output characteristics can be accomplished by the small-signal modeling. Taking PV application as an example, a normal operation for voltage control generally starts from the open-circuit voltage of PV panels *V*oc and stays at operating points where *V*PV > *V*MPP, where *V*MPP is the voltage at the maximum power point (MPP). Based on the

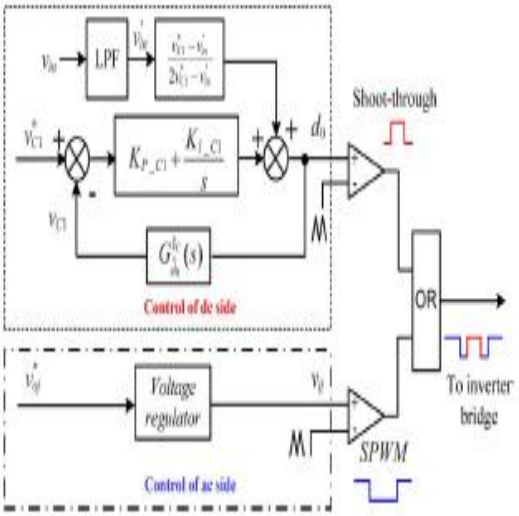


Fig. 6. Two-stage control method of the qZSI for output voltage control.

Linear approximation, a proportional–integral (PI) controller assisted with a feedforward *d*0 is used as the shoot-through compensator. The feed forward *d*0 is determined according to the inherent relationship of *vC*1 and *v*` in in steady state

(16)

Where*v*`in is the input voltage *v*in after a low-pass filter. Based on the small-signal modeling, PI parameters for the *vC*1 control loop can be decided. In order to prevent the clashes between the dynamics of ac and dc sides, the dc-side dynamics should be made considerably slower. This could be supported by having a relatively lower bandwidth in the dc-side voltage loop.

According to the qZSI network specification in Section II (*L* = 500 *μ*H, *C* = 400 *μ*F, *R* = 0.03 Ω, *r* = 0.47 Ω, *D*0 = 0.25, *I*load = 9.9 A, and *V*in = 130 V), the crossover frequencies of the PI controller and low-pass filter are both set to 25 Hz, where *KP*`*C*1 = 1× 10−4 and *KI*`*C*1 = 0.8.

For the ac-side control, traditional methods explored for voltage regulation are applicable to the qZSI. In a three-phase system, fundamental frequency components are commonly transformed to dc components via *d*−*q* transformation, where a simple PI compensator can be applied with good performance.

Another choice is to design the controller in stationary frame. Without *d*−*q* transformation, the designed controller is applicable to single-phase system

too. This paper employs a typical multiloop controller in stationary frame as the voltage regulator,

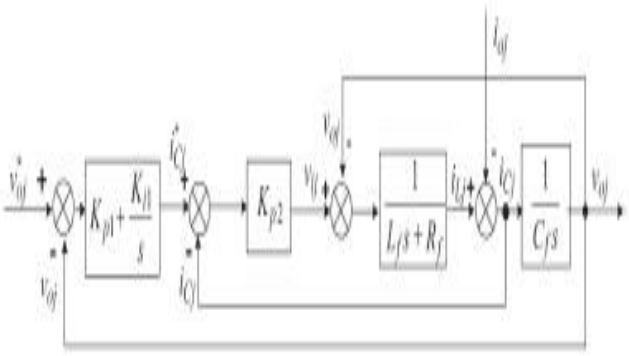


Fig. 7. Control block diagram of the voltage regulator for qZSI.

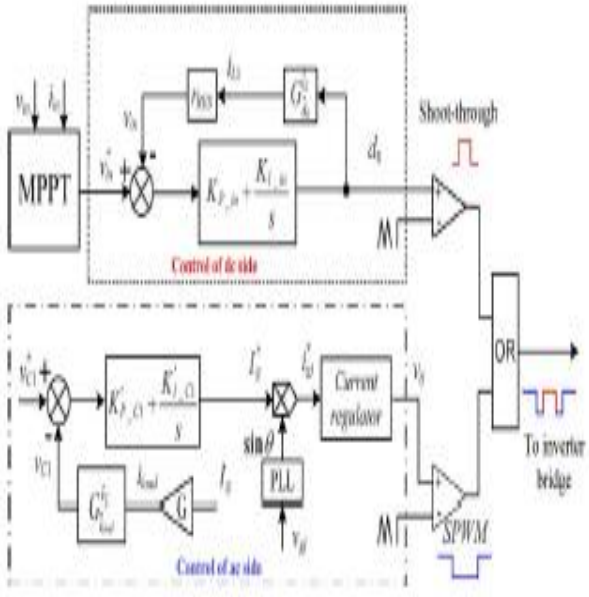


Fig. 8. Two-stage control method for grid-connected-qZSI-based PV power conditioning system.

as shown in Fig. 7. From Mason's gain rule, the closed-loop transfer functions can be obtained, based on which the ac-side controller can be designed properly. In this implementation, *Kp*2 was selected based on the principle of keeping the closed loop gain 0 dB from system output frequency (60 Hz) to half of the switching frequency (5 kHz in this implementation), where *Kp*2 = 30. Considering the time delay $e-sT$ *s* caused by the digital implementation, *Kp*2 would be less in practice to maintain a sufficient phase margin for stable performance. The outer voltage loop control parameters *Kp*1 and *Ki*1 are selected with the compromise that the crossover frequency is low enough to remove the switching harmonics but a sufficiently high bandwidth is retained to have fast response and perfect reference tracking. In this implementation, *Kp*1 is 0.05 and *Ki*1 is 300, where the crossover frequency is 200 Hz and the phase margin is 70◦.

9.2 Controller Design for Output Current Control

Fig. 8 shows the overall diagram of the two-stage control method in grid-connected qZSI, where pulses from control of dc side and that of ac side are combined in the same manner as in the output voltage control mode.

For the ac-side control, capacitor voltage *vC*1 is measured and fed back. The magnitude of the grid current reference *I*g* is generated through a PI compensator according to the error signal of *vC*1. In the case that *v* C*1− *vC*1 is positive, power injected into the grid should be reduced to maintain a constant *vC*1, so negative PI parameters are used here. Along with the phase angle of the grid voltage given by phase-locked loop, the reference of ac current injected into the grid *i*gj* can be obtained.

Since grid current magnitude is proportional to the equivalent load current *i*load in small-signal mode, a coefficient *G* is used to transfer *Ig* to *i*load, which relates to inverter operating condition (e.g., modulation index, shoot-through duty ratio, and the power factor). Consequently, the dynamics of *vC*1 caused by load change can be obtained via transfer function *G*ˆ*vC*ˆ *I* load(*s*),

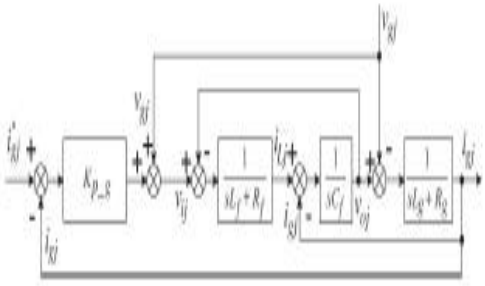


Fig. 9. Control block diagram for output current of qZSI.

as shown in the Appendix. Similar to voltage control mode, *v*C*1 should be selected according to (13)–(15), depending on the specific boost control method engaged. Various control methods for the grid-connected inverter can be applied as the current regulator. This paper employs a conventional method in stationary frame, which is applicable to single-phase system too. It needs to be noticed that, for the proposed three-phase three-wire system, only two controllers are necessary since the third current is given by the Kirchhoff current law. Fig. 9 shows the block diagram of the current regulator, where a current feedback loop, along with grid voltage feed forward, is used. The grid voltage feed forward part guarantees a good disturbance rejection effect. Based on Mason's gain rule, transfer functions of control to output can be derived, according to which *Kp`g* can be decided. In this implementation, *Kp`g* is set to 0.06, the crossover frequency is 1 kHz, and the phase margin is 89◦.

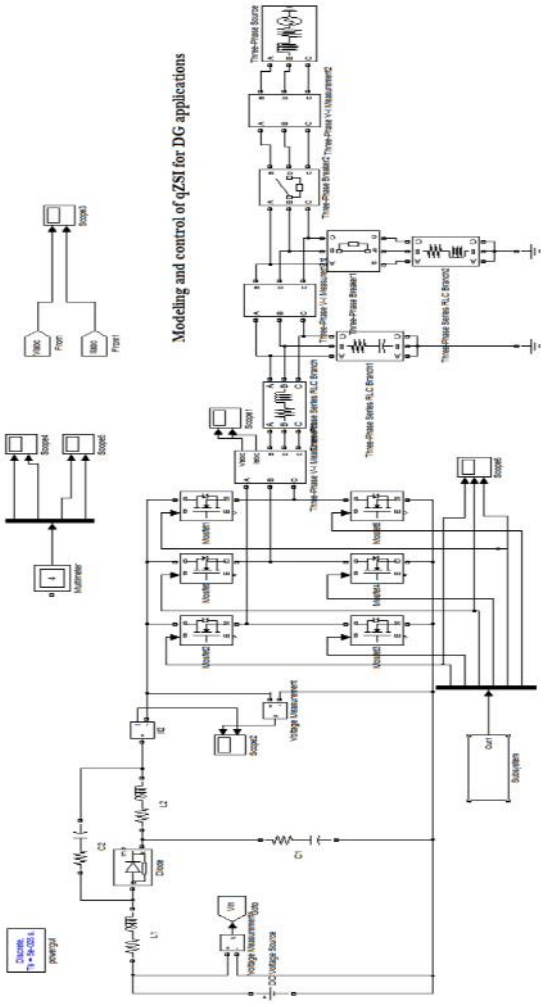
As long as *vC*1 is kept constant by the ac-side controller, reference tracking of input voltage can be achieved at the dc side by adjusting *d*0, referring to the steady-state derivation (11). The reference of the input voltage *v** in of the qZSI is given by output power command, which, in most cases, could be the MPP tracking (MPPT). The PI controller is used to regulate the shoot-through duty ratio *d*0. Through *G* ˆ*I L* ˆ *d*0 (*s*), the variation of *d*0 gives a change on input current *iL*1, which can be further transferred to input voltage by the impedance of the RES *r*RES. Based on the small-signal modeling, PI parameters for the *v*in control loop can be decided. In order to ensure valid operation, PI parameters

of the dc side are selected with relatively slower response compared to the control loop for *v*C1.

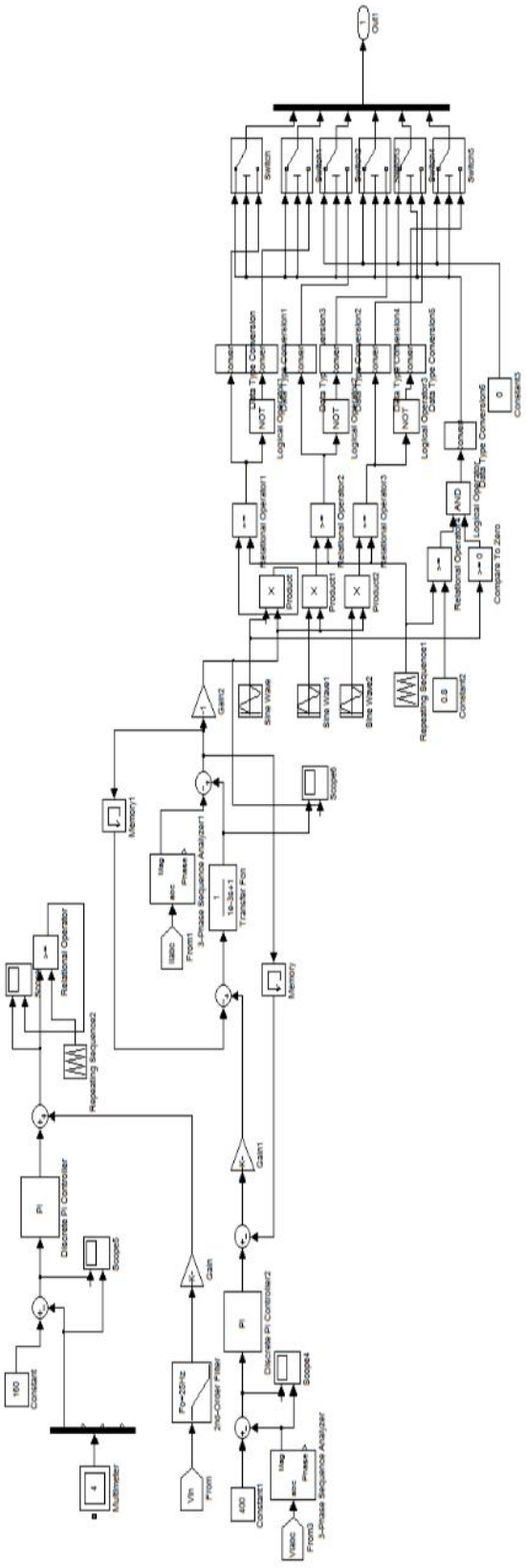
To an end, parameters of PI compensators for the *v*C1 control loop and *v*in control loop are chosen based on the following principles: The bandwidth of the *v*in control loop is lower than that of the *v*C1 control loop, and both of them are lower than that of the current control loop, where $K`P`C1 = -0.1$, $K`I`C1 = -20$, $KP`in = -0.002$, and $KI`in = -0.04$ practically. It should be pointed out that, unlike the output voltage control, a valid operating point in output current control can be located on both sides of *V*MPP. This is because *d*0 is adjusted to track *v*in in the output current control case, instead of regulating *v*C1 for output voltage control. Therefore, MPPT algorithm that sets operating points backward and forward around the MPP can be applied effectively.

IV.SIMUALTION RESUTLS

1 CIRCUIT:

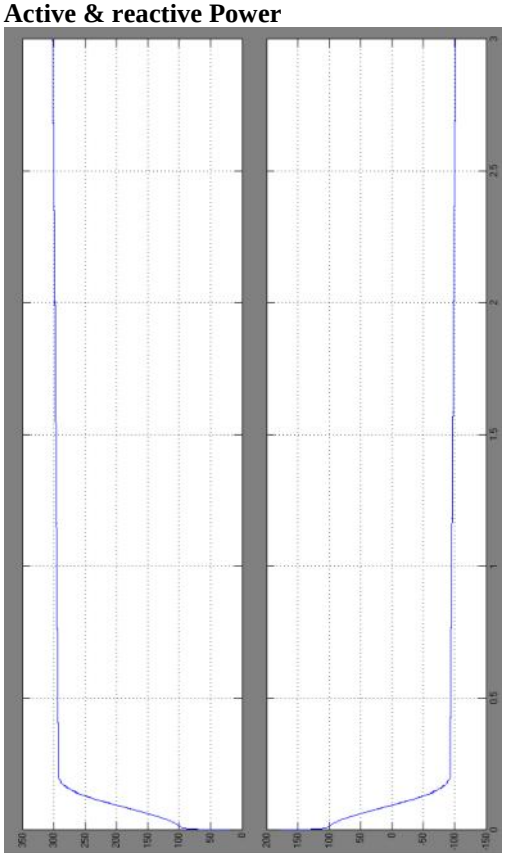


2.Control Circuit:

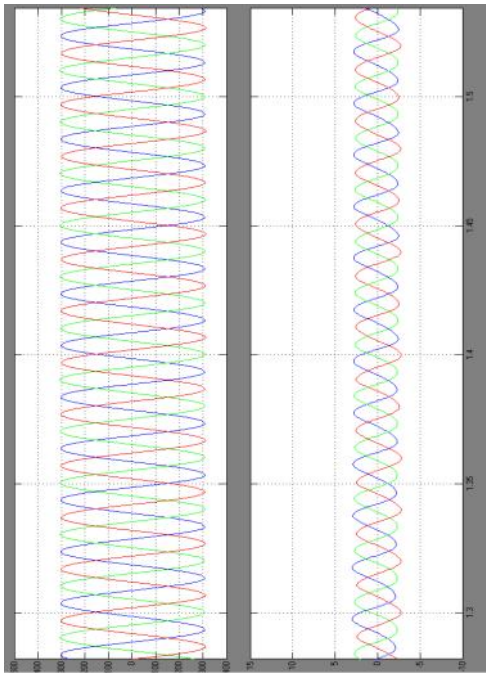


3.WAVEFORMS:

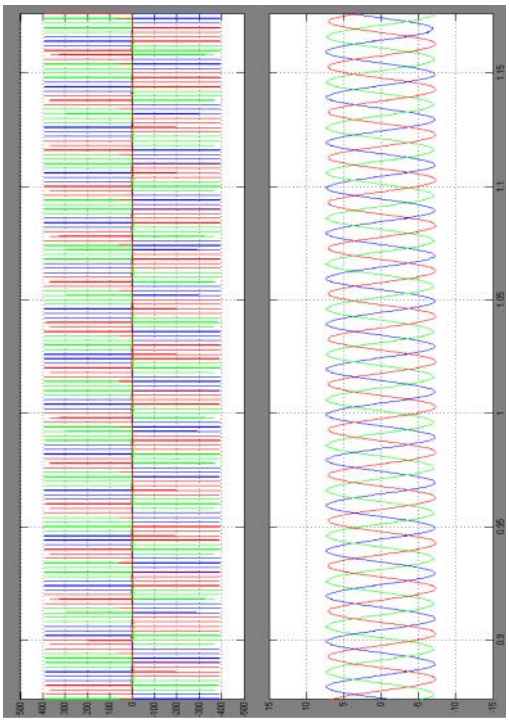
Active & reactive Power



Grid voltages & currents



Inverter output before filtering



CONCLUSION

This paper has emphasized a two-stage control method for the qZSI-based DG. The dynamical characteristics of the qZSI network have been investigated through small-signal analysis. Based on the dynamical model, the two-stage control method for qZSI operating in both output voltage control and current control modes has been presented. MPPT in grid-connected qZSI-based DG is implemented by the proposed controller. Experimental and simulation results confirm the effectiveness of the controller, exhibiting good reference-tracking and disturbance rejection characteristics. Compared to the conventional control of dc-link voltage, control of the capacitor voltage in Z-source/quasi-Z-source network for voltage boost is preferred. This is mainly because the capacitor voltage reference can be set to a certain value at the same time as the minimized voltage stress on switching devices can be achieved. The only drawback of capacitor voltage control approach is that the voltage stress on devices is unapparent. Thus, limitation of *d*0 in dc-side control is necessary to protect from overvoltages on the switching devices.

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