DESIGN OF AN EFFICIENT BYPASSING RELIABLE MULTIPLIER

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Abstract - Digital multipliers are most critical functional units of digital filters. The overall performance of digital filters depends on the throughput of multiplier design. Multiplication may be a heavily used operation in signal process and scientific applications. Multiplication may be a terribly hardware intensive subject and thus we as users area unit largely involved with obtaining low-power, smaller space and better speed. This hold logic reduces the performance will effect on delay. The efficient bypass reliable multiplier is used to reduce the delay. This efficient bypass reliable multiplier design can be applied to digital filter so as to enhance its performance. The verilog language is used for coding, synthesis was done by using Xilinx ISE 13.1

Key Words: Bypass multiplier, hold logic.

I.INTRODUCTION

Day by day IC technology is obtaining additional advanced in terms of style and its performance analysis. A quicker style with lower power consumption and smaller space is implicit to the trendy electronic styles. Unceasing advancement in electronics style technology makes improved use of energy, code knowledge with success, communicate info way more firm, etc. significantly, several of those technologies address low-power consumption to fulfil the necessities of assorted transportable applications. In these application systems, a multiplier could be a basic arithmetic unit and wide employed in circuits that the multiplication method ought to be optimized properly. Multipliers typically have extended latency, huge space and consume substantial quantity of power. Thus lowpower number style has become a very important half in VLSI system style. Everyday new approaches square measure being developed to style low-power multipliers at technological, physical, circuit and logic levels. Since multiplier is mostly the slowest component during a system, the system's performance is decided by performance of the multiplier.

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The AM is a fast parallel AM and is shown in Fig. 1. The multiplier array consists of $(n-1)$ rows of carry save adder (CSA), in which each row contains $(n-1)$ full adder (FA) cells.
Each input is connected to an FA through a tristate gate. When the inputs are $1111_2 * 1001_2$, the two inputs in the first and second rows are 0 for FAs. Because $b1$ is 0, the multiplexers in the first row select $aib0$ as the sum bit and select 0 as the carry bit. The inputs are bypassed to FAs in the second rows, and the tristate gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power consumption is reduced.

II.PROPOSED SYSTEM

In the proposed architecture, the multiplicand or multiplicator to predict the operation using efficient bypass reliable multiplier. The multiplicator and multiplicand follows a normal distribution. The below figure 1 shows the efficient bypass reliable multiplier architecture.

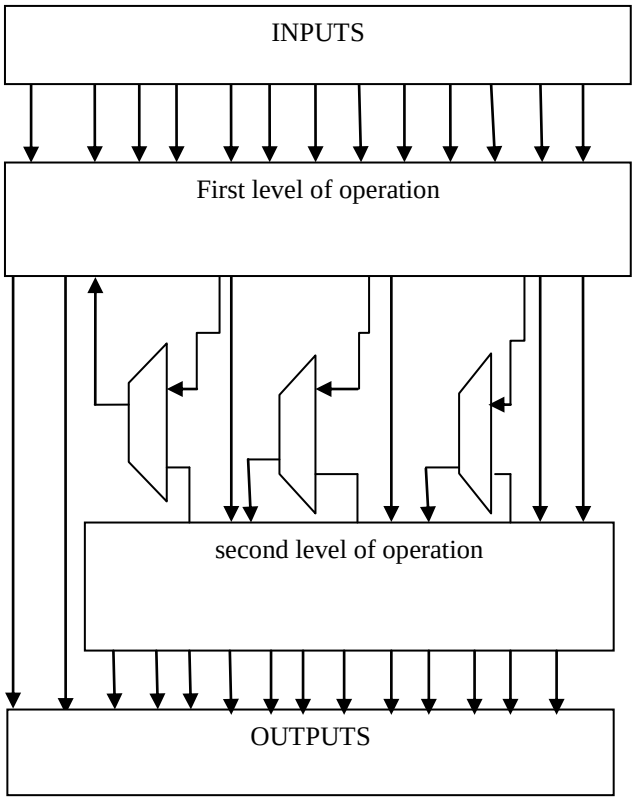

Fig. 1 Efficient Bypass reliable multiplier architecture.

The inputs of the multiplier are multiplicand X and multiplier Y. These two inputs goes under first level of

operation and then goes to second level of operation with mux gives the outputs of multiplier.

Our proposed multiplier design has two key features. First, it is a variable-latency efficient design that minimizes the timing waste of the noncritical paths. Second, it can provide reliable operations even after the aging effect occurs.

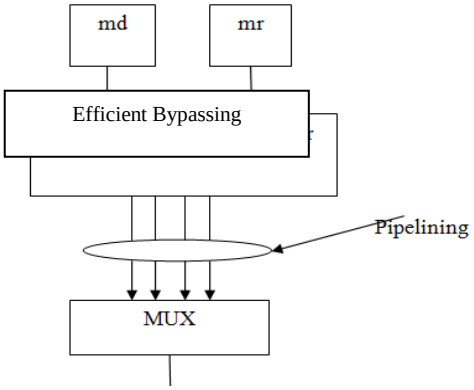

Fig. 2 Block diagram.

Above figure 2 shows the basic block diagram of efficient bypassing multiplier with

MUX family. It consists of two input registers to read two input values. Inputs are passed to the efficient bypassing multiplier and after the completion of operation in efficient bypassing multiplier the partial products are passed to multiplexer. Multiplexer gives the final product depending on the preferences.

The main goal of this paper is to design and implement efficient bypassing multiplier 32×32 multiplier. The experiment results shown below. The below fig 3 shows the RTL schematic of efficient bypass reliable multiplier.

III.RESULTS

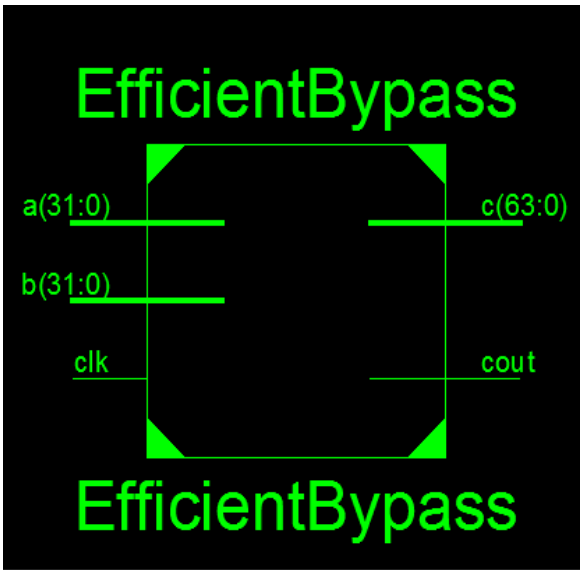

Fig. 3 RTL Schematic.

The figure 4 shows the technical schematic of efficient bypass reliable multiplier.

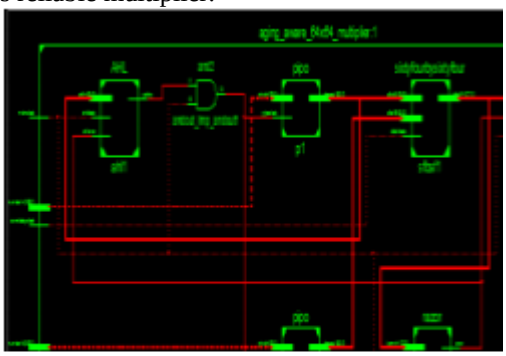

Fig. 4 Technical Schematic.

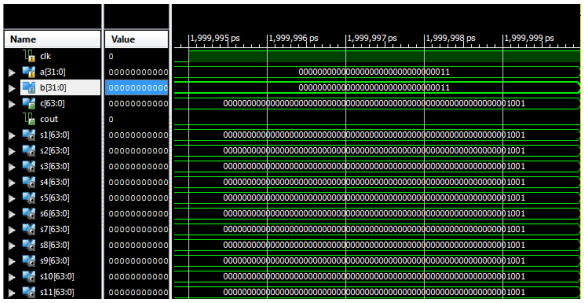

Fig. 5 output waveform.

The above fig shows the output waveform of efficient bypass reliable multiplier. The below tabular form shows the comparison of area and delay for both existed system and proposed system

System	AREA[kb]	DELAY[ns]
Existed	595912	178
Proposed	334756	138.16

IV.CONCLUSION

Multiplication with hold logic reduces the performance will effect on delay. The efficient bypass reliable multiplier is used to reduce the delay. By using proposed system will gives better performance than existed system. The parameters like area, delay and speed are highly positive perform to maintain the system. The delay of the system is reduced so speed is increased.

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