DESIGN AND IMPLEMENTATION OF 16-BIT BAUGH-WOOLEY MULTIPLIER WITH GDI TECHNOLOGY

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ABSTRACT - In this paper we focused upon the Design and Implementation of 16-bit Baugh-Wooley multiplier with GDI Technology. Various electronic devices based on VLSI technology have been of interest to the research community from several decades. These devices have emerged as alternatives to the traditional VLSI technology based on CMOS. These include designs for adders and multipliers. This thesis concentrates on a multiplication of signed number with two's complement form, namely the Baugh-Wooley multiplier. And the tool for this purpose was Xilinx ISE 12.1. We start with the design of XOR gate and Full Adder with the Gate Diffusion Input Technique and due to this technique the count of transistor reduces from 44 as traditional full adder to 18 in number. Thus the whole multiplier architecture was found to be area efficient along with increase in speed and performance. The Baugh-Wooley multiplier with its basic literature review and its Mathematical calculation for 16-bit multiplier was presented with reference to 4-bit architecture as in literature. It can be observed that the circuit consists primarily of several full-adders so a good full-adder solution in Verilog-HDL directly contributes to the efficiency of the Baugh-Wooley multiplier. Thus the full-adder can be realized in Xilinx ISE 12.1. Finally we design in Xilinx and analyze the simulated result for the trade-off such as transistor count, Area etc. The design was found to be efficient than the existing design of multiplier for two's complement numbers.

I.INTRODUCTION

A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. It is built using binary adders. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of partial products, and then summing the partial products together. This process is similar to the method taught to primary schoolchildren for conducting long multiplication on base-10 integers, but has been modified here for application to a base-2 (binary) numeral system. A multiplier is one of the key hardware blocks in most digital signal processing (DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis (Ayman.A et al (2001)). Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design

Algorithms such as FIR, IIR and FFT are required DSP based calculation which solely depends on the design of the multiplier and these are the standard sub-parts of digital processors and also used in ASIC based DSP processors. As many DSP based task which works in real time need to perform multiple tasks in a fast manner with the demise in power along with area. Since due to time complexity the array multiplier has effected from delay having large size of operand and with the complexity in space of O(n2), and requires n2 cells for multiplication and the result will increase in size and power for large operands. As Wallace tree multiplier has a drawback as hardware complexity, need large routing area. So, this technique is not apt for VLSI Design of multipliers. The core use of demise in hardware with Booth can be recombine with Wallace tree for product of half-done and also shrinks the complexity in time of O(log n). For large number of operands, it is the good choice.

Digital multiplier plays an important role in micro controllers and digital signal processors (DSP) which has the MAC (Multiply and Accumulate) unit. As DSP structures seldom need multipliers of differ in size. A generic HDL code is useful to prove these structures. By using this method, the designers can conceive different multipliers of different size by simply changing the operand size factor.

In present scenario, multipliers are playing crucial part in digital signal processing and in many real time applications. As upgrading the technology, researchers involved to design the better multipliers which provide efficient improvements in high performance, near to zero power consumption, minimized area, and regularity of outline

II.SERIAL/PARALLEL MULTIPLIERS

The essential approach for serial/Parallel multiplier circuit is represented below the figure.2. In this the multiplier recognizes the signed or unsigned 2‟s complement numbers and produce them. As in figure, the input y data is functioned in parallel and bit serial can be performed for multiplication. And x data is feed across the multiplier for serial operation. For each and every cycle N numbers of partial products are generated. For each successive cycle, each bit is added to the m*n partial products. The overall outcome accumulated after the n-m cycles, the needed area is n-1 for equal number of M-N. The advantage in hardware of this multiplier is compare to Baugh Wooley multiplier. The architecture represents the 32 bit Shift and Add multiplier for Multiplication of 32 bits. Depending on LSB Bit of multiplier, for every continuous clock, the bits of multiplier succeed to right and checked. If LSB bit is logic one then it acts upon shift operation. And its value is one then multiplicand is further

added to accumulator after that succeeded to right for one bit.

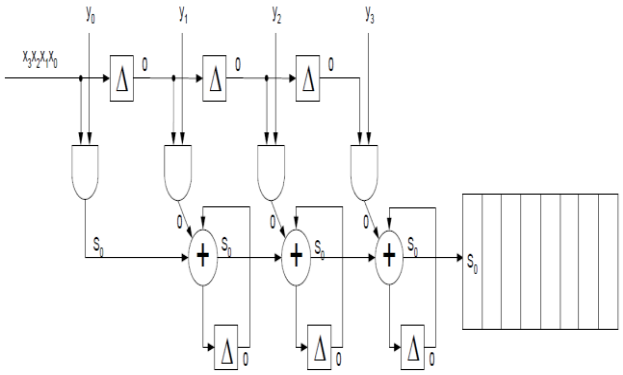


Fig.1 Design of Serial/Parallel Multiplier

After the all 32 bits operation over then the multiplier bits are checked and product to accumulator. The size of accumulator is 2N (M-N), multiplier has N is initially in LSB. In asynchronous circuits, multipliers have more improvements.

III.BAUGH-WOOLEY MULTIPLIERS

The algorithm which is having array multiplication for two"s complement bits is Baugh and Wooley. The focal point of this multiplier is the sign bits of all the multiplicand and multiplier is unsigned or positive. This algorithm is completely designed by using the conventional logic full adders. Here two"s complement numbers multiplied and then finally we get the products as (p0 –p6). The multiplication proposes of Baugh-Wooley Multiplier approach is represented below.

			x	a_3 b_3	a_2 b_2	a_1 b_1	a_0 b_0
			1	$\overline{a_3b_0}$	a_2b_0	a_1b_0	a_0b_0
			$\overline{a_3b_1}$	a_2b_1	a_1b_1	a_0b_1	
		$\overline{a_3b_2}$	a_2b_2	a_1b_2	a_0b_2		
1	a_3b_3	$\overline{a_2b_3}$	$\overline{a_1b_3}$	$\overline{a_0b_3}$			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig.2 Baugh-Wooley multiplier for 4X4 bits

In this report, the research work has been presented for the Xilinx based VLSI design of the 16-bit Baugh-Wooley multiplier with the GDI technique used for the design of Full-adder unit cell. Since the Baugh-Wooley multiplier which were having very significant applications in DSP processors, signal and systems where convolution of signal is required. The authors in various papers shows a traverse approach to system design, through dealings among the algorithm design and core architecture and circuit accomplishment, can capitulate the most significant up gradation in design intricacy. In this work has been showing by the Verilog implementation for system design to obtain the results of various mathematical concepts. The GDI based designing of the multiplier at various CMOS technology level gives various result of improvement in the field of complexity reduction. The optimization of transistor or MOS chips is the major concern in the growing technology in the design of various multiplier architecture with applied algorithms.

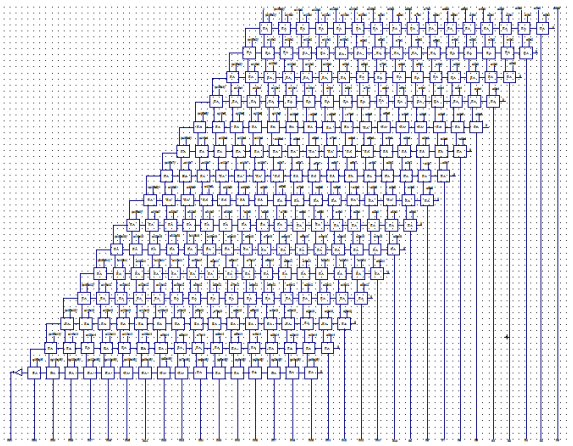


Fig.3 Block Architecture of 16x16 bit Baugh-Wooley Multiplier

IV.RESULTS

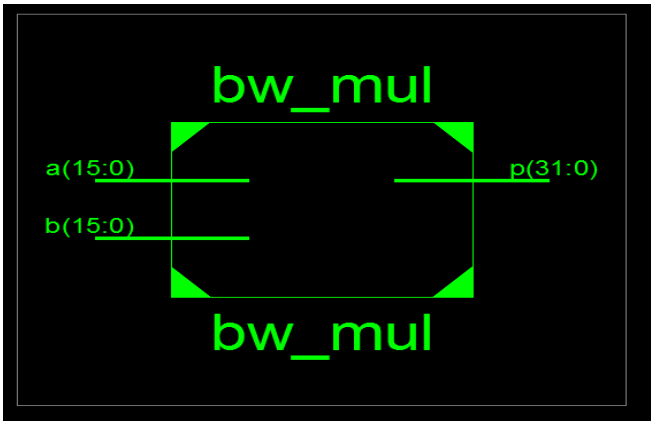
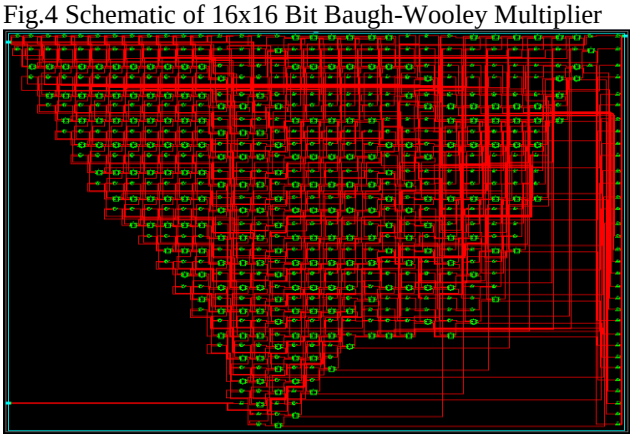


Fig.4 Schematic of 16x16 Bit Baugh-Wooley Multiplier



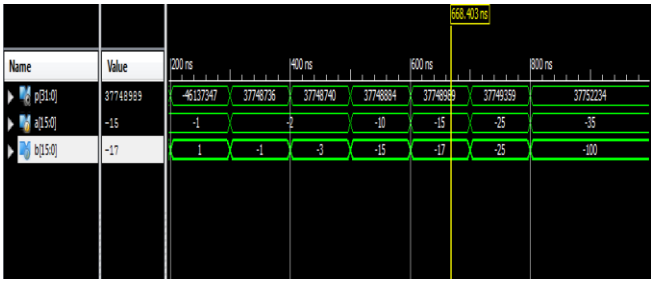


Fig. 5 Output Waveform for some random number taken in test bench

CONCLUSION

Even after many years after its proposal, multipliers have innumerous problems in all levels of the design flow, like the layout floor planning and some fault problems due to delay paths. This report presented the design of a 16- bit Baugh Wooley Multiplier using the GDI based Adder‟s. The basic steps were the Formulation of discrete partial product terms using the and/nand gate Boolean expressions. Then, the multiplier was assembled using the GDI based Full Adder generated in the procedure of designing.

In this report, we have showed the design of the 16-bit Baugh-Wooley multiplier with GDI based Full Adder in Xilinx. The designs are based on some results in GDI logic. The designs have been simulated and results show that the proposed design has low area as well as low transistor Count.

This report also proposed a design methodology for multiplier circuits through the simulation of the full-adder based on Gate Diffusion Input technique. The Simulation Results from Xilinx ISE 12.1 is obtained. The layout is adopted from the RTL Generated from the ISE one used to balance the pipelined circuits. The proposed design methodology will speed up and facilitate the design of large GDI-based digital circuits much more. A design example proves the correctness and accuracy of this design methodology.

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