Design and Implementation of A Multiplier Using N.S. Gate

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ABSTRACT:
The model of computing in which the computational progression is reversible or to some extent inverting is entitled reversible computing. In the VLSI the logic gates are and, or, ex-or are not reversible. Here the 4*4 reversible gate designs called NSG. The purpose of NSG is to implement in all logical Boolean operations. The vital reversible gates that perform reversible logic synthesis are Feynman gate, toffoli gate, fredkin gate, peres gate etc., and some of other reversible gates. By using these reversible N.S gate we make a multiplier that gives very efficient o/p. The used software is Xilinx 13.1, family sparton 6, device XC6SLX4, and package TQG144, preferred language VHDL.

INTRODUCTION

The Feynman gate is simulated for future computing techniques for low ultra power digital circuits and quantum computers. We want to build a linear reversible function by using 2*2 Feynman gates and Inverters. When this occur means if a=0 &q=b then a=1 and q=b'.

Toffoli gate is called as CCNOT gate. Full form of CCNOT =controlled-controlled-not gate. It has 3 bit inputs and outputs. If first two bits are set, it inverts the third bit otherwise all the bits same way.

The controlled not gate is a quantum gate. That is an essential in the component of construction. It consists of two qubits the Cnot gate flips the second qubit if the first qubit the reliability of the cnot operation was to be in order of 90%.

The Proposed NS Gate i.e. "NSG" can singly be implemented in all logical Boolean operations. Reversible logic has publicized possibilities to have widespread purpose in upcoming emerging promising technologies such as quantum computing, optical computing, quantum dot cellular automata in addition to ultra low power VLSI circuits. we are using 4*4 reversible gate called as NSG.

PROPOSED SYSTEM

The reversible adder circuits proposed till now, NS gate is better than the previous full-adders design. The proposed full adder using NS Gate requires only one reversible gate (one NS Gate) and the NS Gate produces only 2 garbage outputs while performing operations like full adder, full subtractor, half adder and half subtractor. Apart from the other reversible gates proposed till now NS Gate can also singly perform the function of a full subtractor, half adder and half subtractor with only two garbage outputs now we design an multiplier.

The below fig. 2 shows the block diagram of N.S gate multiplier. The working of a recorder is to record the data and it will store as dynamic memory element.

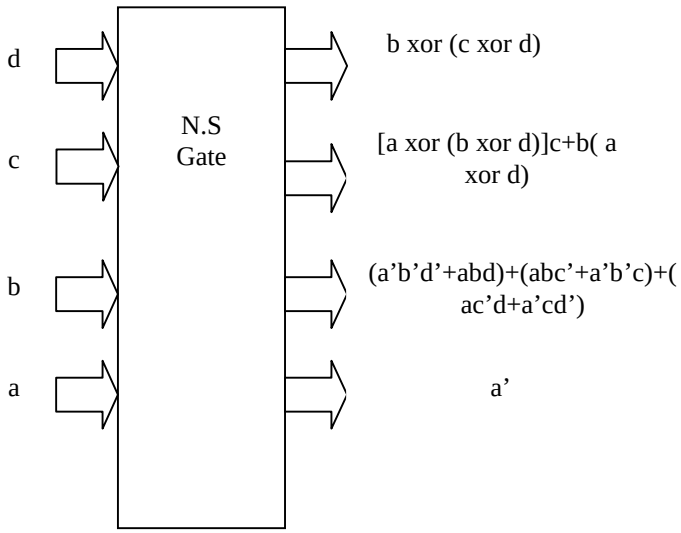

Fig. 1 N.S GATE

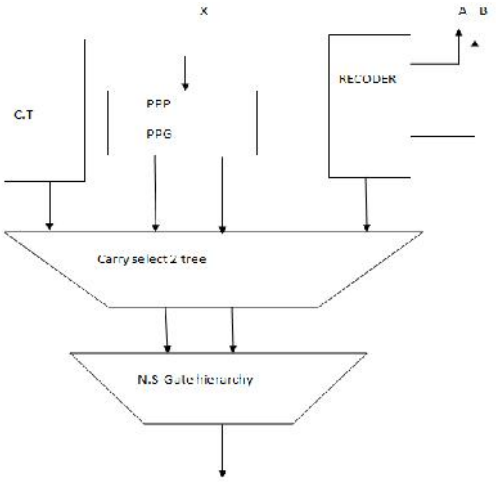

Fig. 2 BLOCK DIAGRAM

The above propagate PPP and generate PPG are used for the pre processing. The carry select tree is used to design hierarchy by using N.S gate. The hierarchy design gives the preference as per operation and gives high performance multiplier design.

RESULTS

The proposed NS Gate multiplier architecture is implemented in VHDL (Very High Speed Integrated Circuited Hardware Description Language) furthermore the FPGA synthesis is done using Xilinx ISE Design Suite 14.S.The below fig. 3 shows the RTL schematic of N.S. gate

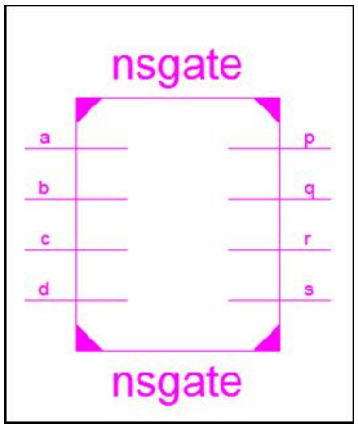

Fig. 3 RTL Schematic

The N.S gate consists of four inputs and four outputs. The below fig. 4 shows the output graph of N.S. gate. The inputs are a, b, c, d and outputs are p, q, r, s.

Fig. 4 output graph of N.S.gate

The below fig. 5 shows the technical schematic of N.S gate multiplier. It consists of LUT's, IBUF, OBUF.

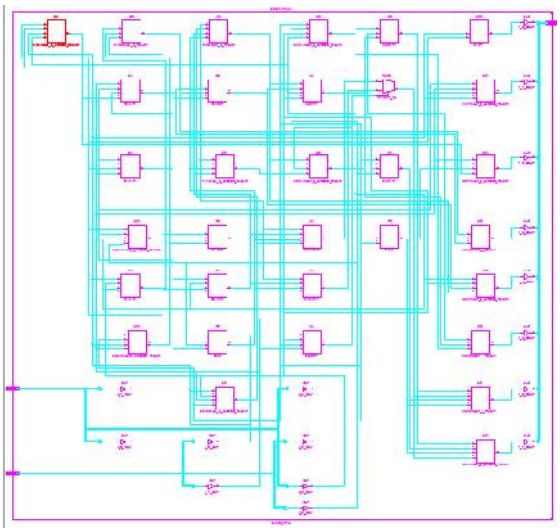

Fig. 5 Technical Schematic

The below fig. 6 shows the output graph of N.S. gate multiplier.

Fig. 6 output graph of N.S.gate multiplier

Now, the simulation result of the most important and prominent purpose of the proposed multiplier.

CONCLUSIONS

The purpose of NSG is to implement in all logical Boolean operations. The vital reversible gates that we use reversible logic with garbage outputs reduce the unused operation. By using these reversible N.S gate we make a multiplier that gives very efficient o/p than general multiplier design.

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