Design An Energy Efficient P.D Encoder And Decoder

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ABSTRACT:
The area and power has become an important design criterion in modern system designs, especially in portable battery-driven applications. A significant portion of total power dissipation is due to the transitions of the gates. There are many encoding schemes in the literature that achieve a huge reduction in transition activity on the instruction address bus. However, on data and multiplexed address buses, none of the existing schemes consistently achieve significant reduction in transition activity. In this paper, P.D encoder and decoder are proposed that significantly reduce transitions on these buses without adding redundancy in space or time. Also, for applications with tight delay constraints, configurations with minimal delay overhead while still achieving significant reduction in transition activity are proposed. The proposed schemes are then compared with the existing schemes. It is seen that on an average, the reductions achieved by P.D encoder and decoder techniques better than existed technique.
Key words*: Network on Chip; Low power; Data encoding; Coupling capacitance; Power analysis*

I.INTRODUCTION

In accordance with Moore‘s law density of transistors doubles every 18 months and currently we all know that there are millions of FETs on a single chip is known as VLSI. Integrating these FETs combine together to perform set of operations and applications such as DSP, Communications, Robotics and medical filed. Continuous improvements in semiconductor technology make it possible that a whole computing system comprising processors, memories, accelerators, peripherals, etc. can now be integrated in a single silicon die. This trend has been favoured thanks to the definition of new design methods which stress the reuse of pre-designed and pre-verified modules in the form of intellectual properties (IPs or cores).

We focus on technique aimed at reducing the area and delay dissipated by the network links. In fact, the area and delay dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales. In particular, we present a set of data encoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both the switching activity and the coupling switching activity on links of the routing paths traversed by reducing the number of gates.

In our P.D encoding technique, all possible input symbols are assigned codes. For every input symbol, the corresponding encoding is transmitted and the codes are adapted based on the current input symbol and current encodings.

II.PROPOSED WORK

The proposed encoding architecture, the body flits are grouped in *w* bits by the NI and are transmitted via the link. In our approach, spare bits of the link are used for the inversion bit, which indicates if the flit traversing the link has been inverted.

The modified encoding logic *E*, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion with less number of gates. To make the decision, the previously encoded flit is compared with the current flit being transmitted. We will reduce the number of transitions between the most frequently accessed address ranges by assigning them the codes with minimal Hamming distance. Both the encoder and decoder initialize with the same symbols in the same positions. Once a symbol is processed, the encoder outputs its position and then the symbol is shifted. All the codes that from the position 0 until the position of the symbol being coded are moved to the next higher position. This simple scheme assigns codes with lower values for more redundant symbols. The proposed block diagram of decoder is shown below Fig. 2.

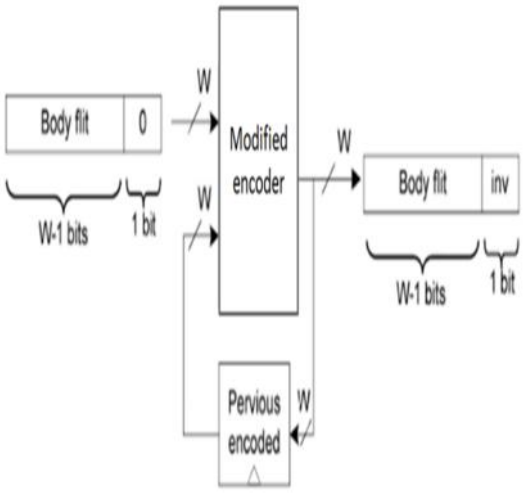

Fig. 1 Proposed Encoder Block Diagram

As we observe that the architectures are shown for both encoder and decoder are similar but the inputs and outputs are different. The encoder input is body flit and spare bit, the body flit is the input and spare bit is used for inversion bit at the output of encoder similar to that an body flit of data is also produced. The output of encoder is given to

input as decoder the final output is produced at body flit at decoder output block.

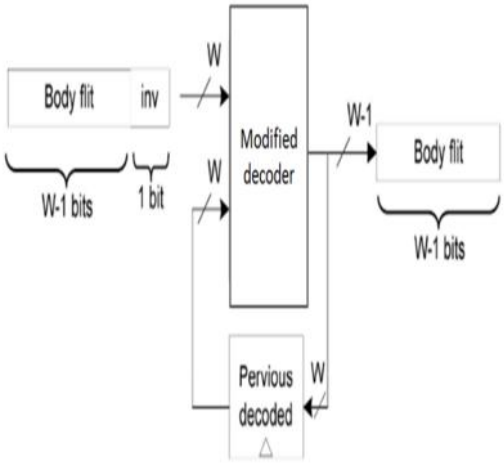

Fig. 2 Proposed Decoder Block Diagram

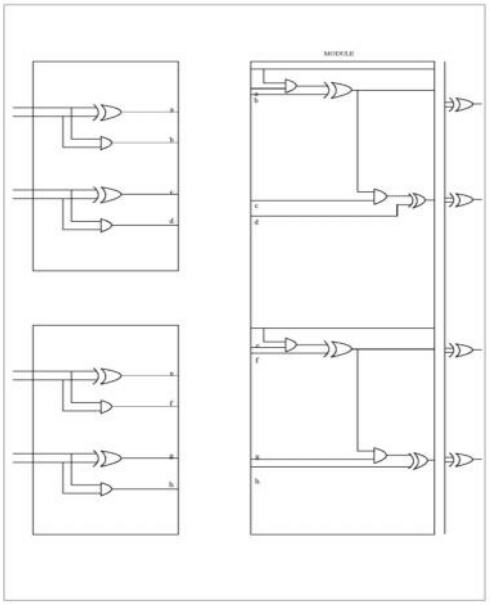

Fig. 3 Architecture of Encoder

The proposed encoder architecture is shown in fig. 3. Here the number of gates using in the module are redused 4 OR gates & 4 AND gates used in T1,T2 blocks. Only 4 AND gates ,4 OR gates used in module block. 4 XOR gates are used at the output.

Here 2 AND gates, 3 OR gates are redused then the power consumption is also redused. The speed of the operation will be incresed. The encoder output is given to input as decoder then the final output will displayed. The partial architecture of encoder and decoder is shown in figures. The decoder architecture is shown below fig. 4.

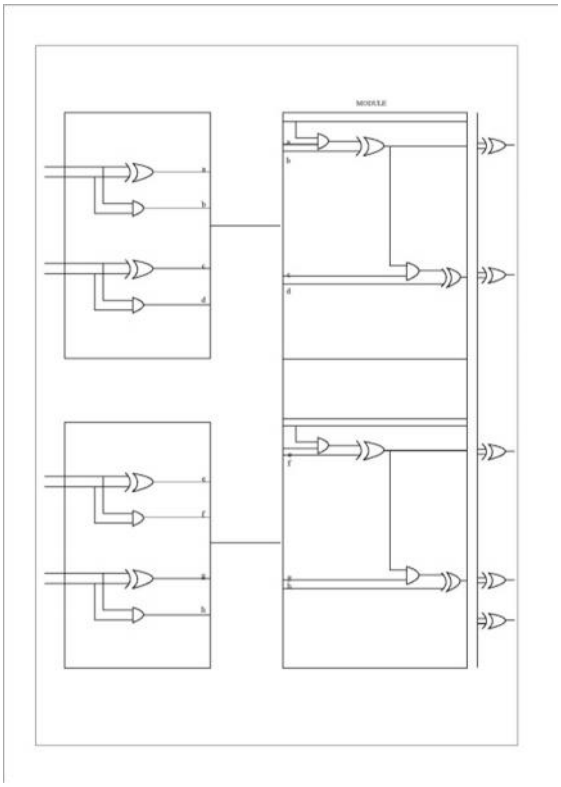

Fig. 4 Architecture of Decoder

III.RESULTS

Fig. 5 Output waveforms

The output waveforms are shown in fig 5 and comparison table is shown below.

Table 1: Comparison table

	EXISTED SYSTEM	PROPOSED SYSTEM
DELAY	16.8ns	15.5ns
MEMORY USED	187760kb	187504kb

CONCLUSION

P.D encoder and decoder are proposed that significantly reduce transitions on these buses without adding redundancy in space or time. Also, for applications with tight delay constraints, configurations with minimal delay overhead helps to achieved significant reduction in transition activity are proposed. The proposed schemes are then compared with the existing schemes. It is seen that on an average, the reductions achieved by P.D encoder and decoder techniques better than existed technique.

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