Design An High Performance Dual Logic Level Multiplier

1. SHAIK MAHAMMAD GOUSE,PG Student,2.BHUKYA BALOJI NAIK, Assistant Professor, 1,2.E.C.E Department SAI TIRUMALA N.V.R ENGINEERING COLLEGE

ABSTRACT: This paper presents the design an dual logic level [D.L.L] multiplier for 32*32 bit number multiplication. Modern computer system is a dedicated and very high speed unique multiplier. Therefore, this paper presents the design an dual logic level multiplier. The proposed system generates M,N and interconnected blocks. By extending bit of the operands and generating an additional product the dual logic level multiplier is obtained. Multiplication operation is performed by the dual logic level is efficient with the less area and it reduces delay i.e., speed is increased.

Keywords: D.L.L, partial products, dual level logic unit.

INTRODUCTION

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low-power VLSI system design. There has been extensive work on low-power multipliers at technology, physical, circuit and logic levels. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system.

Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully parallel.

The high speed multipliers and pipelined multipliers are used for digital signal processing (DSP) applications such as for multimedia and communication systems. High speed DSP computation applications such as Fast Fourier transform (FFT) require additions and multiplications. The conventional modified Booth encoding (MBE) generates an irregular partial product array because of the extra partial product bit at the least significant bit position of each partial product row. Therefore papers [4] presents a simple approach to generate a regular partial product array with fewer partial product rows and negligible overhead, thereby lowering the complexity of partial product reduction and reducing the area, delay, and power of MBE multipliers. But the drawback of this multiplier is that it function only for signed number operands.

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The multiplier array consists of $(n-1)$ rows of carry save adder (CSA), in which each row contains $(n-1)$ full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation.

The gates in the dual logic level [D.L.L] multiplier are always active regard of input logics. In, dual logic level [D.L.L] multiplier design is proposed in which the operations are disabled if the corresponding bit in the multiplicand is 0.

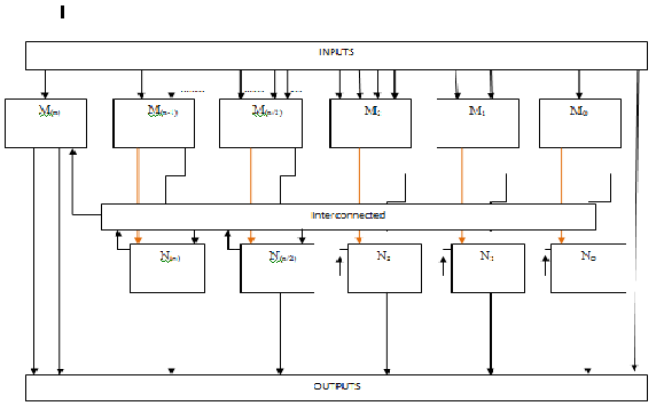

Fig. 1 4 x 4 HIGH PERFORMANCE DUAL LOGIC LEVEL MULTIPLIER

PROPOSED SYSTEM:

Fig. 1 shows a N×N dual logic level [D.L.L] multiplier, it can be seen that the M0,M1,…Mn done their operations and the outputs are passed to interconnected

Block and N-Block simultaneously. Depends on the preference of operation the dual level logic gives the N-block output to interconnected block and vice versa.

Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit. The above fig. 1 shows the 4*4 high performance dual logic level multiplier reduced the timing waste occurring in traditional circuits that use the critical path cycle as an execution cycle period. The basic concept is to execute a shorter path using dual logic. Since most paths execute in a cycle period that is much smaller than the critical path delay. The same architecture is extended up to 32*32 bits.

Dual logic level widely been adopted in multipliers since it can reduce the number of partial product rows to be added, thus reducing the size and enhancing the speed of the reduction tree. The least significant bit position of each partial product row encoding, leading to an irregular partial product array and a complex reduction tree. Therefore, the dual logic level

multipliers with partial product array produce a very high speed.

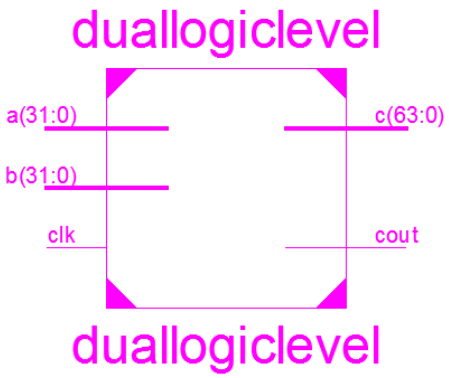

Fig. 2 R.T.L Schematic

The above fig. 2 shows the R.T.L schematic of high performance dual logic level multiplier and fig. 3 shows the technical schematic one of the LUT block of high performance dual logic level multiplier.

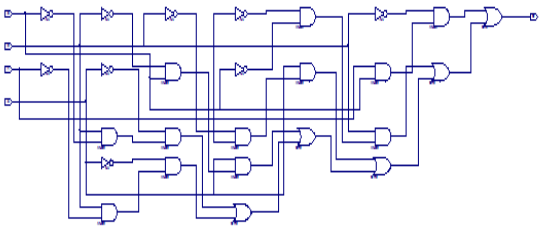

Fig. 3 LUT in technical Schematic

The below figure 4 shows the output waveform of 32*32 bit dual logic level multiplier.

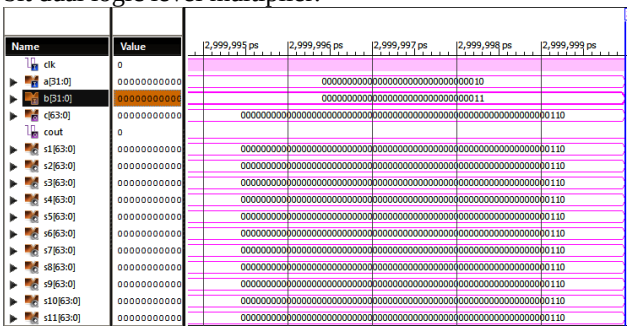

Fig. 4 OUTPUT Waveforms

The below table 1 shows the comparison of existed system and proposed system with area and delay

System/parameter	Area[kb]	Delay[ns]
Existed System	382256	410
Proposed system	304820	130

Table.1 comparison table

The above comparison table shows that area of the proposed system is less than existed system and delay is also efficient. The graphical representation of parameters is shown below

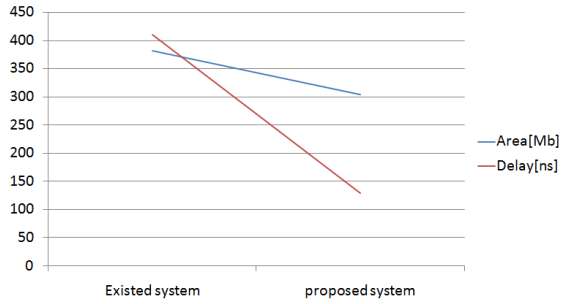

Fig. 5 Comparison Graph

The blue line shows the area and the other shows the delay.

CONCLUSION

The proposed system generates M, N and interconnected block. The each block consists of gates and the row in the architecture is lesser than existed multiplier. By generating an product with dual logic level multiplier is obtained. Multiplication operation is performed by the dual logic level unit is better performance than existed multiplier. The required hardware and the chip memory reduces and it reduces delay i.e., speed is increased.

REFERENCES

[1] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and miimization of pMOS NBTI effect for robust naometer design," in *Proc. ACM/IEEE DAC*, Jun. 2004, pp. 1047–1052.

[2] H. Abrishami, S. Hatami, B. Amelifard, and M. Pedram, "NBTI-aware flip-flop characterization and design," in *Proc. 44th ACM GLSVLSI*, 2008, pp. 29–34

[3] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesis of digital circuits," in *Proc. ACM/IEEE DAC*, Jun. 2007, pp. 370–375.

[4] A. Calimera, E. Macii, and M. Poncino, "Design techniqures for NBTItolerant power-gating architecture," *IEEE Trans. Circuits Syst., Exp. Briefs*, vol. 59, no. 4, pp. 249–253, Apr. 2012.

[5] K.-C. Wu and D. Marculescu, "Joint logic restructuring and pin reordering against NBTI-induced performance degradation," in *Proc. DATE*, 2009, pp. 75–80.

[6] Y. Lee and T. Kim, "A fine-grained technique of NBTI-aware voltage scaling and body biasing for standard cell based designs," in *Proc. ASPDAC*, 2011, pp. 603–608.

[7] M. Basoglu, M. Orshansky, and M. Erez, "NBTI-aware DVFS: A new approach to saving energy and increasing processor lifetime," in *Proc. ACM/IEEE ISLPED*, Aug. 2010, pp. 253–258.

[8] K.-C. Wu and D. Marculescu, "Aging-aware timing analysis and optimization considering path sensitization," in *Proc. DATE*, 2011, pp. 1–6.

[9] K. Du, P. Varman, and K. Mohanram, "High performance reliable variable latency carry select addition," in *Proc. DATE*, 2012,
pp. 1257–1262.

[10] A. K. Verma, P. Brisk, and P. Ienne, "Variable latency speculative addition: A new paradigm for arithmetic circuit design," in *Proc. DATE*, 2008, pp. 1250–1255.